

A 2 GHz Highly Linear Downconversion Mixer in 0.18- μm CMOS

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Abstract—This paper describes a 2 GHz CMOS active balanced downconversion I/Q mixer in a TSMC0.18- μm process for a WCDMA receiver. The mixer achieves a conversion gain of 16 dB and a double side band (DSB) NF of 13.8 dB. The mixer's IIP3 is 12.12 dBm. It consumes approximately 5 mA of current from a 1.8-V power supply. The 12.12 dBm IIP3 fulfils the UMTS requirements for a mixer design.

I. INTRODUCTION

CMOS RF integrated circuits (RFIC) for wireless applications in the 2 GHz frequency range has grown tremendously during the last few years. The prospect of system level radio integration with low external components for cellular handset has led to increased interest and research of direct conversion mixer. The mixer, as a nonlinear circuit by definition, is the most critical analog building block in the front-end receiver. It provides frequency translation from RF to the intermediate frequency (IF) called “down-converter”, or from IF to RF called “up-converter”.

CMOS mixers with gate length of 0.18 μm or below open up the possibility of low power consumption in a RF front-end IC applications. One typical receiver architecture applied in a WCDMA receiver is shown in Fig. 1. In the downconversion, the frequency translation process will generate some unwanted spurious signals to degrade the signal-to-noise ratio (SNR), the linearity becomes an important factor of mixer. In most of the front-end transceivers the linearity of the mixer affects the overall linearity. Therefore, linear mixer is very important in the design of front-end transceivers. The design of mixers forces many compromises between conversion gain, local oscillator (LO) power, linearity, noise figure, port-to-port isolation, voltage supply, and current consumption. In CMOS mixers research area, a passive linear mixer [1] can have a very high IIP3 (around 40 dBm) but its NF is very high (around 30 dB). Such a high NF will limit the SNR of a front-end. Using current mode multiplication technique [2], CMOS active mixer may be designed but with the sacrifice of the lower conversion gain. To overcome this low conversion gain, a very high gain of low noise amplifier (LNA) is required to minimize the effect of noise degradation on the overall receiver design. This work is for a 2 GHz CMOS active downconversion quadrature mixer design for a WCDMA receiver. Here, we

will concentrate mainly on linearity, gain and noise figure in our downconversion mixer design.

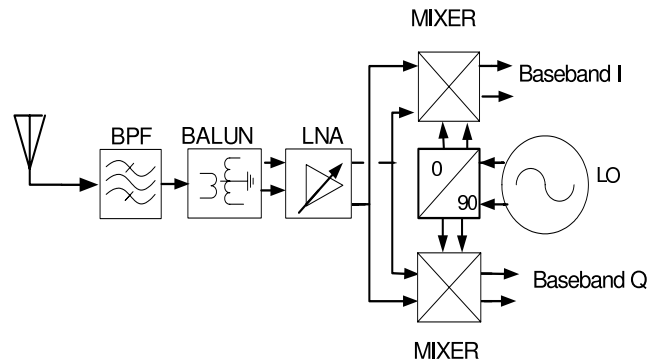


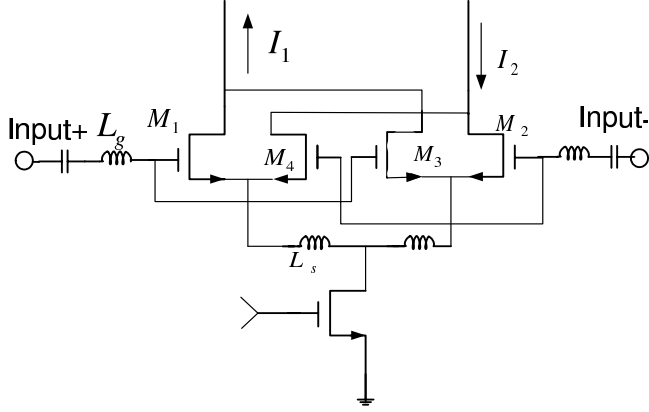
Fig. 1. Front-end of a direct downconversion receiver

This paper describes the design of a 1.8-V active downconversion mixer in a 0.18 μm CMOS process. The prototype design will be suitable to integrate with an LNA [3] for a monolithic WCDMA front-end receiver design. The rest of the paper is organized as follows. Section II describes the principle is used to dedicate the design. Design details is described in section III and section IV presents the simulation results of the sample. Finally, section V derives the conclusion.

II. PRINCIPLE

A. g_m cell technique

In the Fig. 2, the devices M_3 and M_4 form a g_m cell [4] with input transconductors for enhancing linearity of the mixer. The aspect ratios of the matching transistors M_3 and M_4 are different than the matching transistors M_1 and M_2 . In this configuration, each input differential pair behaves a reasonably linear transconductance over a small specified input voltage range. Thus, the overall transconductance is the sum of the individual offset transconductance and can be made roughly constant over an almost arbitrary large range of input voltage. Obviously, we must be careful about the added input capacitance of this cell to the common source input impedance for input matching and noise optimization.


 Fig. 2. Schematic of g_m cell

III. CIRCUIT IMPLEMENTATION

The proposed double balanced I/Q downconversion mixer without bias circuit is shown in Fig. 3. The mixer comprises

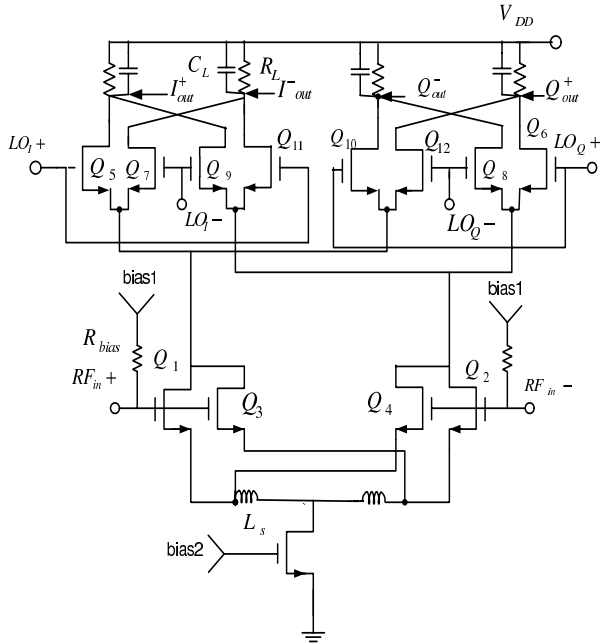


Fig. 3. Schematic of the mixer

differential pairs driver stages (Q1-Q4) and four differential switching quad (Q5-Q12). The transconductors are inductively degenerated to achieve higher linearity. We use devices Q_3 and Q_4 at the input transconductors, Q_1 and Q_2 , respectively for further linearity improvement as explained in section II. The driver stage amplifies the RF signals to compensate for the attenuation due to switching process, and to reduce the noise contribution from the switching quad. The two I and Q

mixers are resistively loaded because of reducing flicker noise at outputs. Four mixers gates are attached each driver stage.

At the transconductor output, the signal is split into I and Q paths inside the mixer. Two independent I and Q LO signals (off-chip) are applied to create quadrature baseband paths. The transconductor output current splits between I and Q paths such that all of the transconductor input current goes to the I branch at the the instance that the Q branch core is in its conducting state, and vice versa. Therefore, each switching pair will not have any current at the balanced point and the noise generated by the switching core transitions may be reduced periodically.

The load capacitors are chosen such that it works as low pass filters with cutoff frequency at 45 MHz for removing the strong out-of-band signals from the input to the baseband filters.

IV. CONVERSION GAIN, NF AND IIP3

The conversion gain of a double balanced mixer can be approximated by

$$A_C = 20 \log \left(\frac{2}{\pi} (g_m R_L) \right) \quad (1)$$

where g_m is the transconductance of Q_1 and Q_2 . From 1, we can see that a higher gain can be obtained by increasing the g_m or the load resistance.

The NF of a double balanced mixer can written by [5]

$$NF = 10 \log \left(2 + \gamma \frac{4R_L I}{\pi A} + \gamma \frac{2R_L I}{(V_{gs} - V_t)} \right) \quad (2)$$

where I is the bias current of the input device and A is the amplitude of the LO signal. From 2, it can be seen that the relative contribution of the switches to the transconductance FET is $2(V_{gs} - V_t)/(\pi A)$ for short channel devices. As the gate over-drive bias on the transconductors approaches the LO amplitude, the swiches and transconductance stages contribute comparable noise at the mixer output.

The IIP3 of a double balanced mixer can be approximated as

$$IIP3 = 10 \log \frac{4}{3} \frac{(V_{gs} - V_t)(1 + \Theta(V_{gs} - V_t)^2)(2 + \Theta(V_{gs} - V_t))}{\Theta} \quad (3)$$

where Θ is the modulation factor. From 3, the interesting observation is that linearity improves with increasing the over-drive voltage, $(V_{gs} - V_t)$ of the input trasconductors but for sacrificing higher power consumption.

V. SIMULATION RESULTS

We simulate our mixer with the cadence SpectreRF simulator. Figures 4 to 6 show simulation results of the mixer. We find that the mixer achieves a conversion gain of 16 dB and a NF of 13.8 dB. As two-tone testing, two tones are located at 2.09 GHz and 2.08 GHz, respectively. Fig. 6 illustrates IIP3 measured to be 12.12 dBm. Table I summarizes the performance of the mixer and compares the performace of this mixer with the one in [6].

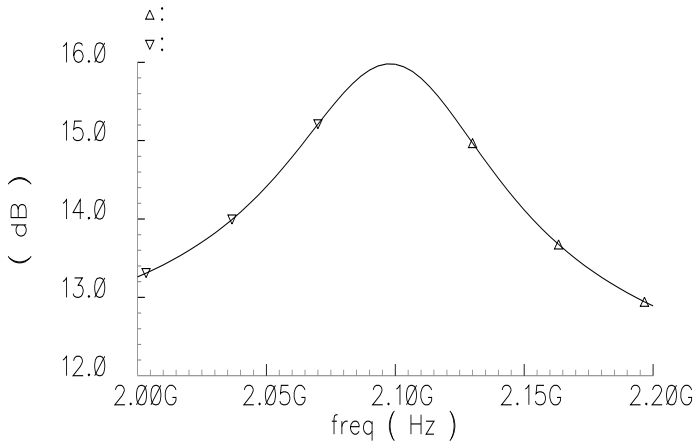


Fig. 4. Conversion gain of the mixer

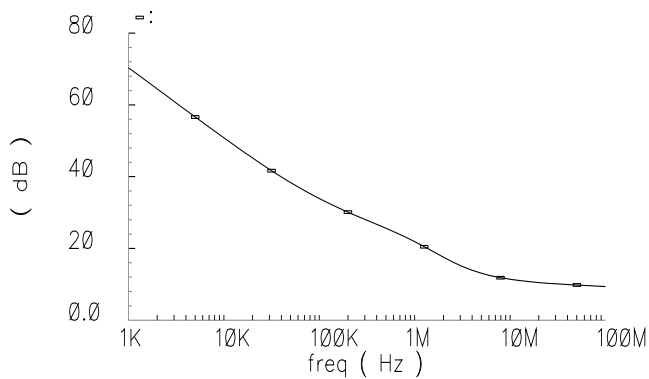


Fig. 5. NF (DSB) of the mixer

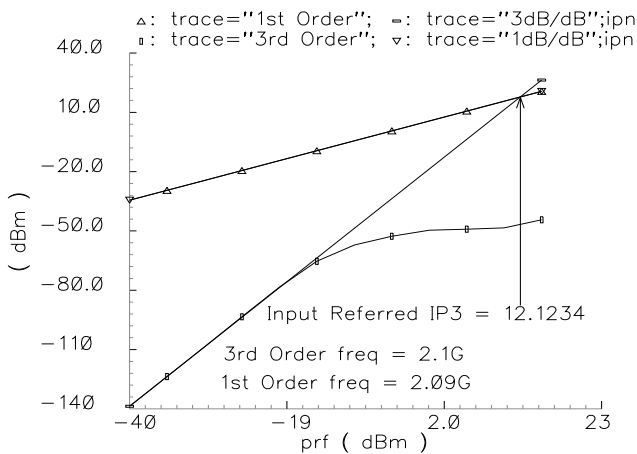


Fig. 6. IIP3 of the mixer

TABLE I
PERFORMANCE SUMMARY OF THE MIXER

Parameters	This work	[6]
Center frequency (GHz)	2.1	2.1
Current (mA)	5	2×6
Conversion Gain (dB)	16	12
NF (dB)	13.8	20.5
IIP3 (dBm)	12.12	13
LO Power (dBm)	-2	N.A
LO to RF feedthrough (dB)	-132	N.A.
Supply (V)	1.8	1.5
Power Consumption (mW)	9	2×9
Technology	TSMC 0.18 μm	0.13 μm

VI. CONSTANT g_m BIASING

Performance of the mixer such as gain, NF and linearity depends primarily on the transconductance of the transistors Q_1 - Q_4 . Taking into account process spread, supply voltage variation 10% and temperature variation (-45°C to 85°C), the worst case performance are: NF = 25 dB, gain = 7 dB and IIP3 = 7 dBm at a supply voltage of 1.8-V and with a current consumption of 6 mA.

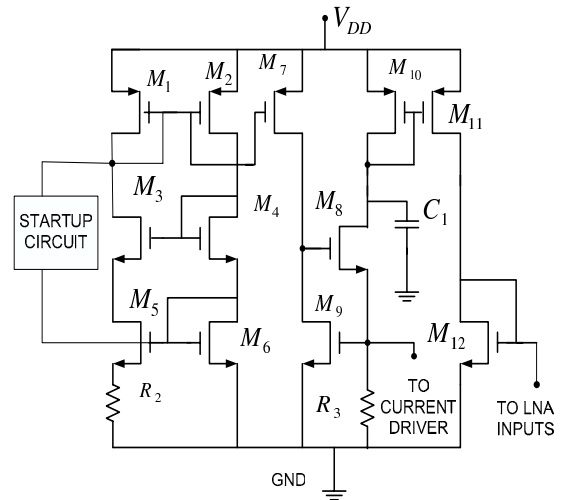


Fig. 7. g_m bias cell

Better circuit performance can be obtained using constant g_m bias circuit [7]. Fig 7 illustrated the biasing circuit for the mixer. In this circuit, a bias current that makes the transconductance, g_m , proportional to a reference conductance,

$1/R2$. The transistor M_5 is much wider than M_6 so that it operates on a very small over-drive voltage. The positive feed-back loop implemented by the current mirror formed by $M_1 - M_4$ ensures that both M_8 and M_9 conduct the same current. The driver of the mixer intercepts the bias current via a current mirror formed by $M_8 - M_9$. To make the current through M_9 proportional to V_{th} , we choose M_9 wider than M_8 . This current provides the bias current for mixer input devices through M_{12} , so that all bias voltages track V_{th} , thus providing a measure of stability.

The biasing circuit stabilizes the mixer amplification. Taking into account process spread, supply voltage variations 10% and temperature variation (-45°C to 85°C), the worst case performance are: NF = 18 dB, gain = 15 dB and IIP3 = 10.5 dBm at a supply voltage of 1.8-V and with a current consumption of 5.5 mA.

VII. CONCLUSION

This paper presents a 2.1 GHz mixer in a TSMC $0.18\mu\text{m}$ CMOS process. The mixer achieves an IIP3 of 12.12 dBm. Operating at 1.8-V supply voltage, the circuit provides a conversion gain of 16 dB. In the noise response, the mixer acquires of 13.8 dB noise figure. The high linearity (IIP3) and low NF fulfill the requirements for a UMTS mixer design.

Thus, this integrated Mixer can be used to achieve direct downconversion in WCDMA front-end which requires RF designers to design fully integrated, low noise, highly linear and low power consumption architecture for SoC applications.

ACKNOWLEDGMENT

The authors would like to thank Texas Instruments for their support in conducting this project. The authors also would like to thank Steve Bybik and Patrick Roblin for their invaluable suggestion on this work.

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