# MIT Lincoln Laboratory's Low Power, High Performance, Fully Depleted SOI CMOS Process Technology*

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## Abstract

Fully depleted silicon-on-insulator (FDSOI) offers several performance advantages when compared to bulk CMOS for deeply scaled device applications, including: near-ideal subthreshold swing, reduced parsitic capacitances, and enhanced harsh-environment resistance. FDSOI-based device technologies (Ultra-thin Body, Dual-gate, and FinFET) are now the leading candidates for end-of-roadmap CMOS fabrication.

MIT Lincoln Laboratory (MIT-LL) has been working aggressively on FDSOI technology since 1994 for use in low-power, high-performance applications. The MIT-LL FDSOI technology was first introduced in 1996 as a 0.25 μm process. The current 180-nm process provides unloaded ring oscillator stage delays of <20 ps at 1.5 volts, and offers a ~6x reduction in power, for the same performance, when compared to a 0.18 μm bulk CMOS technology. Using the FDSOI technology, 5 different DARPA-sponsored "multiproject" runs containing over 150 different circuits from industrial, educational, and government organizations have been fabricated and characterized. In addition, chips designed and fabricated in the technology for NASA were space qualified on-board the Deep-Space-1 spacecraft as part of the *Low Power Electronics Flight Experiment*. Using strong-phase-shifting 248-nm optical lithography, MIT-LL has been extending the FDSOI technology to the sub-50-nm gate length range and has demonstrated gate structures down to 9-nm gate lengths. Recent development is focused on enhancing the RF performance of the technology for use in RF frontends and mixed signal applications.

This talk will provide an overview of the FDSOI technology development activities at MIT-LL. Topics to be covered include FDSOI device/circuit performance, and the application of FDSOI to harsh environments and 3D circuit integration.

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**Brief Bio**:
Craig L. Keast received the B.A. degree from Hamilton College, Clinton NY, and the S.M., E.E. and Ph.D. degrees in Electrical Engineering and Computer Science from the Massachusetts Institute of Technology, Cambridge MA. He is the Leader of the Advanced Silicon Technology Group and Director of the Microelectronics Laboratory at MIT Lincoln Laboratory.