

# A 1.2V 2.4GHz Integrated Direct Downconversion Receiver Front-End

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**Abstract**— This paper presents a low-power, low-voltage radio frequency (RF) receiver front-end implemented in a 0.18 $\mu$ m CMOS process that is intended for 2.4GHz wireless applications. It includes a single-ended low-noise amplifier (LNA) with on-chip spiral inductors and a passive switching direct downconversion mixer. The LNA has a simulated noise figure of 0.76 dB and power gain of 12.9 dB. With a -30dBm RF input and a 0.45V LO signal, the mixer has a simulated noise figure of 7.8dB, conversion gain of -2.2dB, 1-dB input compression point of -8 dBm, input third-order intercept point of 14.4 dBm. This chip is in process for fabrication.

**Index Terms**—Direct Downconversion, LNA, Switching Mixer

## 1. Introduction

BECAUSE of advancements in RF CMOS circuits, devices and passive elements in the last decade, it is possible to develop an RF system-on-chip (SoC)[1] that integrates RF, analog and digital circuits completely for wireless communications. Although the advent of SiGe technology has been a hot topic in the last a few years, rapid progress of scaled CMOS technology has put standard CMOS process in a favorable role in RF fabrications [2]-[4] because of its low-cost essence.

The most widely used RF receiver architecture is a so-called superheterodyne architecture [4], which can provide sufficiently low noise figure (NF). However, this architecture requires an image rejection filter, an intermediate frequency (IF) filter, and at least two LOs, which not only adds to receiver size, but also increases power dissipation. In contrast, a direct downconversion architecture eliminates the image rejection filter and the IF filter, which allows a highly integrated, low-cost and low-power realization [4].

Fig. 1 shows the typical front-end block diagram of a direct downconversion receiver. In order to reduce the noise figure of the overall system, not only the noise performance of the LNA needs to be optimized, but the mixer also should have low NF and adequate conversion gain. On the other hand, the conversion gain should not

need to be too large otherwise a strong signal may saturate the output of the mixer and reduce its power gain.

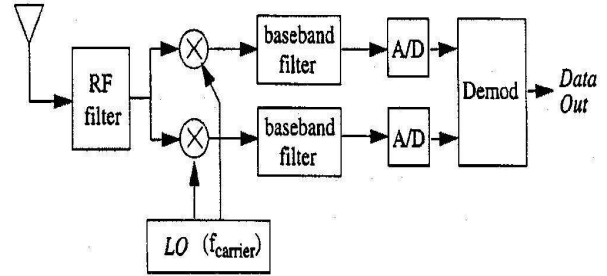


Fig. 1. Block diagram of direct downconversion receiver

A passive switching mixer is described in this paper. The advantage of it over a traditional Gilbert mixer is that the bias currents in the transistors are zero, leading to a low flicker noise[5], which is a significant design aspect in direct downconversion architecture.

In Section II, the noise performance of the LNA is examined, and a new architecture of the LNA is proposed. In Section III, the switching mixer is described. In Section IV, simulation results are provided. Finally, conclusions are drawn in Section V.

## 2. Low Noise Amplifier

The noise performance of a radio frequency communication system is determined by a LNA, which takes advantage of high linearity and sufficient gain to overcome the next stage noise while not to overload the following stages. Inductive source degeneration is the most prevalent method used in LNA designs, because it offers the possibility of achieving the best noise performance of any architecture [2]. A proposed cascode LNA with inductive source degeneration is shown in Fig. 2. It has an intrinsic capacitance  $C_d$  in parallel to the gate capacitance of the amplifying transistor, as well as an interstage inductor between the two stages. For this LNA, its input impedance is [5],[6]:

$$Z_{in} = j\omega L_t + \frac{1}{j\omega C_t} + R_t + \frac{g_{m1}}{C_t} L_s \quad (1)$$

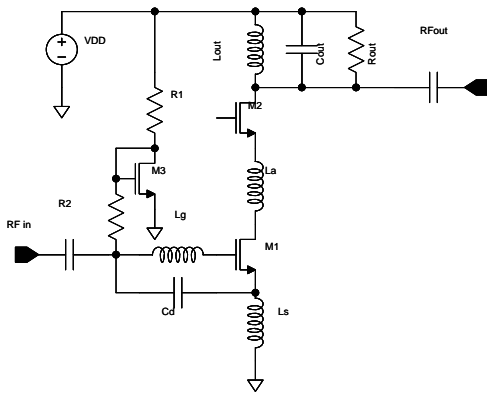


Fig. 2. Proposed LNA architecture

Where:

$$L_t = L_g + L_s \quad (2)$$

$$C_t = C_{gs1} + C_d \quad (3)$$

$$R_t = R_g + R_l \quad (4)$$

$$R_g = R_o \frac{1}{3n^2} \cdot \frac{W}{L} \quad (5)$$

$C_{gs1}$ : Gate-to-source capacitance of M1

$g_{m1}$ : Transconductance of M1

$R_g$ : Effective gate resistance [7]

$R_o$ : Sheet resistance of the gate polysilicon

$n$ : Number of fingers of M1

$R_l$ : Parasitic resistance of  $L_g$  and  $L_s$

At the resonance frequency:

$$f_o = \frac{1}{2\pi\sqrt{L_t C_t}} \quad (6)$$

The input matching condition is:

$$R_s = R_t + g_{m1} \frac{L_s}{C_t} \quad (7)$$

The quality factor for the input circuit is then:

$$Q = \frac{1}{2\pi f_o \left[ R_s + \left( R_t + g_{m1} \frac{L_s}{C_t} \right) \right] C_t} \quad (8)$$

$$= \frac{1}{4\pi R_s f_o C_t} \quad (9)$$

And the unity gain frequency is:

$$f_T = \frac{g_{m1}}{2\pi C_t} \quad (10)$$

Then the noise factor of the LNA can be shown to be

$$F = 1 + \frac{R_t}{R_s} + \gamma g_{d0} R_s \left( \frac{f_o}{f_T} \right)^2 \quad (11)$$

Where:

$g_{d0}$ : zero-bias drain conductance of M1

$\gamma$ : bias-dependant factor that, for long channel devices, satisfies:

$$\frac{2}{3} \leq \gamma \leq 1 \quad (12)$$

It has been found that the dominant term in (11) is the last term, and this arises from channel thermal noise [2]. By scaling down the width of M1,  $g_{d0}$  can be reduced, which implies better noise performance and less power dissipation, provided  $f_T$  is maintained. However, scaling down reduces  $C_{gs1}$ , if  $C_d$  is not added, which in turn results in an increase of  $L_t$  to maintain a constant resonance frequency according to equations (6), (2) and (3). Adding  $C_d$  in parallel with  $C_{gs1}$  not only keeps  $C_{gs1}$  small, which means less gate induced current noise, but also minimizes parasitic effects of  $L_g$  and  $L_s$ [6].

Another step is to design the common-gate stage. The common-gate input impedance is given by[8]:

$$Z_{in2} = \frac{1}{g_{m2} + j\omega C_{gs2}} \quad (13)$$

Traditionally, no matching is taken into account between the common-source stage and the common-gate stage for cascode LNA design. But because both the input impedance of the common-gate stage and the output impedance of the common-source stage are capacitive, it is desirable to add a series inductor  $L_a$  between the two stages to improve the matching[10]. Since power gain is improved by adding this inductor, the Miller capacitance effect will be more significant in the first stage, and the overall noise figure will be improved thanks to better power transfer.

The width of M1 and M2 is  $90\mu\text{m}$ , and  $C_d$  is  $160\text{fF}$ .  $R_1$ ,  $R_2$  and M3 provide biasing for M1, while  $R_{out}$ ,  $L_{out}$  and  $C_{out}$  form the output matching network. The four on-chip spiral inductors are simulated using ASITIC[9].

### 3. Switching Mixer

In typical active Gilbert-type mixers, the RF signal is represented in the form of current instead of the RF voltage itself. The V-I conversion is realized by multiplying it with a square-wave version of the local oscillator. In order to avoid the V-I conversion problem, an alternative is to switch the RF signal directly in the voltage domain. Since CMOS transistors are excellent switches themselves, high-performance passive switching

mixers can be realized effectively with CMOS technology.

A simple double-balanced passive switching mixer is shown in Fig. 3, which consists of four transistors in a bridge configuration. The four transistors operate as switches connecting either the RF signal or the inverse of the RF signal to the output terminal driven by the local oscillator signal.

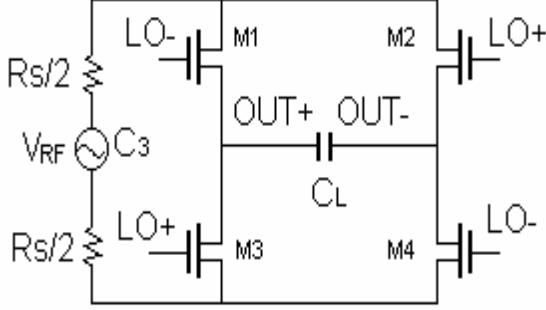


Fig. 3. A simple double-balanced CMOS switching mixer

A general expression of the output of the mixer is given in [5], which is expressed as the product of three time-varying components and a scaling factor:

$$v_{OUT}(t) = v_{RF}(t) \cdot \left[ \frac{g_T(t)}{g_{Tmax}} \cdot m(t) \right] \cdot \left[ \frac{g_{Tmax}}{g_T} \right] \quad (14)$$

where  $g_T(t)$  is the time-varying Thevenin-equivalent conductance as viewed from the output port, and  $\overline{g_{Tmax}}$  and  $\overline{g_T}$  are the maximum and average values, respectively, of  $g_T(t)$ . The mixing function  $m(t)$  is defined by:

$$m(t) = \frac{g(t) - g(t - T_{LO}/2)}{g(t) + g(t - T_{LO}/2)} \quad (15)$$

where  $g(t)$  is conductance of each switch and  $T_{LO}$  is the period of the LO drive. It can be observed that the mixing function has no DC component and has only odd harmonic content because of its half-wave symmetry.

A practical switching mixer used in this front-end is shown in Fig. 4.  $C_1$  and  $L_1$  provide an impedance transformation,  $L_3$  and  $C_3+C_L$  form a parallel bank which acts as a lowpass filter. Because of the absence of DC bias current in this mixer, the flicker noise is absent, which makes it particularly valuable for direct downconversion receivers.

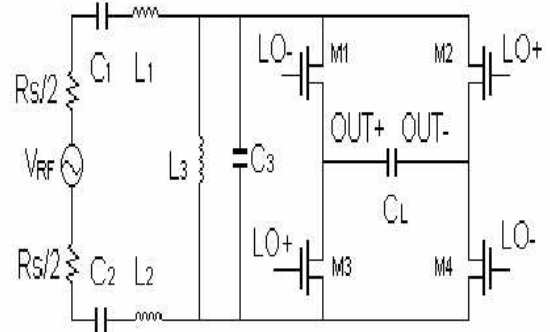


Fig. 4. Proposed switching direct downconversion mixer

## 4. Simulation Results

The proposed LNA and switching mixer circuits are implemented with a  $0.18\mu\text{m}$  CMOS process. For the LNA, power gain and noise with various  $L_a$  values are shown in Fig. 5 and Fig. 6, respectively. It can be found out that when  $L_a$  is increased from  $1\text{ nH}$  to  $5\text{ nH}$ , the power gain is increased from  $17\text{ dB}$  to  $24.5\text{ dB}$ , the noise figure is improved from  $0.81\text{ dB}$  to  $0.76\text{ dB}$ . However, because of the Miller capacitance of  $C_{gd2}$ , the input reflection coefficient becomes worse. Taking these issues as well as the layout into consideration, a  $3.72\text{ nH}$   $L_a$  is chosen. After post-layout simulation, the scattering parameters of the LNA are shown in Fig. 7, and the noise figure is shown in Fig. 8.

For the switching mixer, a  $2.45\text{GHz}$   $0.45\text{V}$  square wave LO signal is used. Two RF tones of  $2.42\text{GHz}$  and  $2.43\text{GHz}$  are applied at the input of the mixer with equal power levels to perform input third order intercept point analysis. Power levels of both tones are swept from  $-30\text{ dBm}$  to  $20\text{ dBm}$  to observe the first order and third order nonlinearity behavior, which is shown in Fig. 9.

Performance of both the LNA and the switching mixer is summarized in Table 1 and Table 2, respectively. It can be seen that the most important advantage of this front-end design is its low-voltage, low-power dissipation and low-noise property. Fig. 10 shows the chip layout of the LNA and the switching mixer that is in process of fabrication.

## 5. Conclusion

A low-power, low-noise design of  $2.4\text{GHz}$  CMOS integrated RF front-end consisting of a low noise amplifier and double-balanced switching mixer for direct downconversion receiver is presented. Excellent noise performance and good linearity have been shown through post-layout simulation.

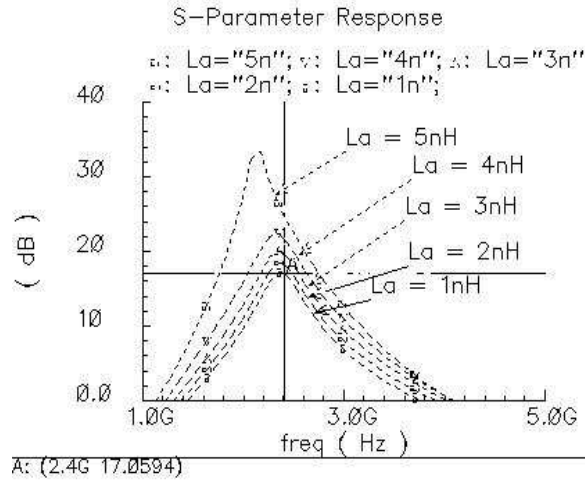


Fig. 5. Power gain of the LNA vs. La

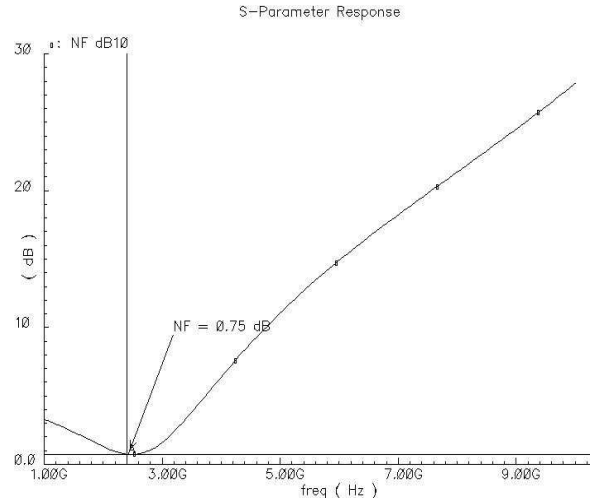


Fig. 8. Noise figure of the LNA

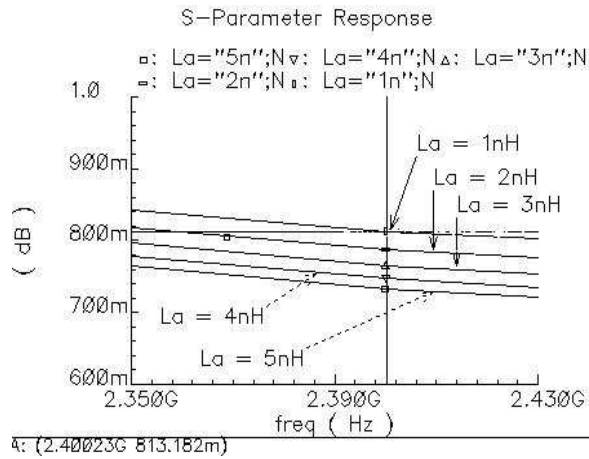


Fig. 6. Noise figure of the LNA vs. La

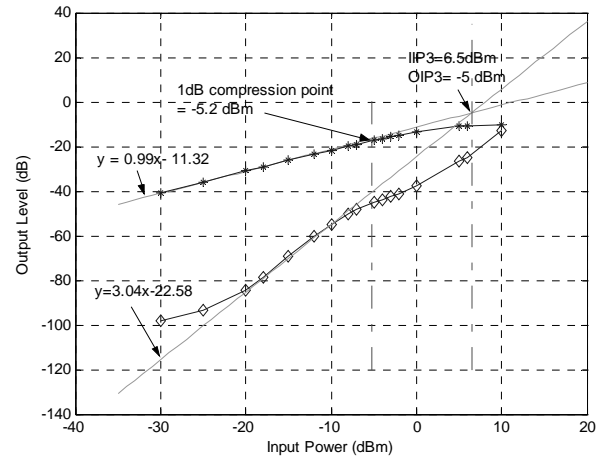


Fig. 9. 1-dB compression point and input third-order intercept point of the switching mixer

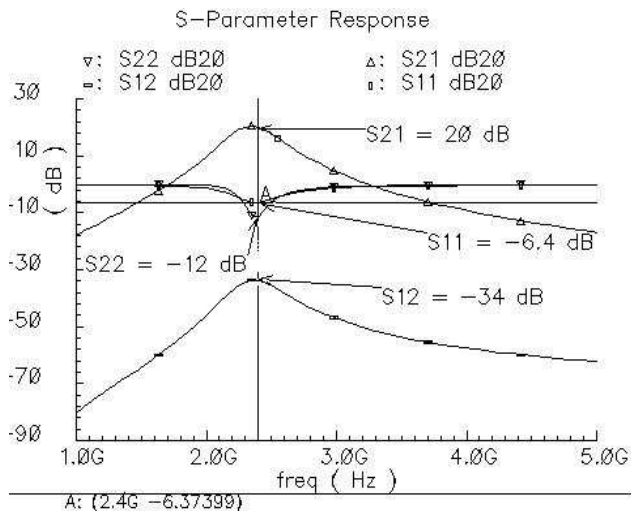


Fig. 7. Scattering parameters of the LNA

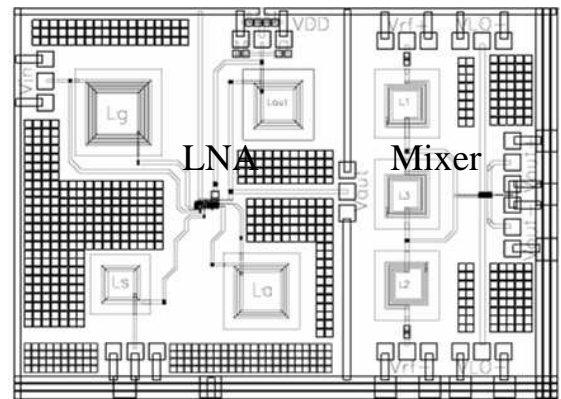


Fig. 10. Layout of the LNA and the switching mixer

Table 1. LNA performance summary

Process	0.18 $\mu$ m 1P6M
Supply voltage	1.2V
Operation frequency	2.4GHz
Power dissipation	2.8 mW
Noise figure	0.75 dB
Power gain	20 dB
S11	-6.4 dB
S12	-34 dB
S22	-12 dB

Table 2. Switching mixer performance summary

Process	0.18 $\mu$ m 1P6M
IF frequency	0
LO frequency	2.45GHz
LO voltage	0.6V
Noise figure	8.8 dB
Conversion gain @ -30 dBm	-2.2 dB
1dB compression point	-5.2 dBm
IIP3	6.5 dBm
OIP3	-5 dBm

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