

Radiation Hardness of Ultra Low Power CMOS VLSI

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Abstract

An Ultra Low Power (ULP) CMOS process instantiated at a commercial U.S. foundry can produce high performance microcircuits which operate at a 500 mV supply, which dramatically reduces dynamic power consumption. In addition to ultra low power performance, the ULP process and circuit design provides an enhanced Total Ionizing Dose radiation performance compared to the baseline CMOS process. Application of proven Hardness By Design techniques further provides immunity to Single Events Effects that are produced in the natural space environment, making the radiation tolerant ultra low power microcircuits highly applicable to spacecraft applications.

1. Introduction

The goal of the University of Idaho's (UI) Ultra Low Power (ULP) Program is to develop a Complementary Metal Oxide Semiconductor (CMOS) Very Large Scale Integration (VLSI) technology that is capable of producing microelectronic devices that operate reliably at voltage levels significantly lower than those targeted in the 2000 update to the Overall Roadmap Technology Characteristics (ORTC) of the 1999 International Technology Roadmap for Semiconductors (ITRS), while maintaining operating speed characteristics that are comparable to contemporary commercial processes. The ULP target operating voltage matches the ITRS targets for the year 2011.

As the dynamic power consumption of CMOS devices is directly proportional to the square of the operating voltage, aggressive scaling of operating voltage yields very significant reductions in power consumption for electrically active circuits. Operating CMOS circuits at

low voltage does however increase susceptibility to "soft errors" that occur when ambient energetic particles strike the junctions of the semiconductor device. Neutrons have been shown to produce Single Event Upsets (SEUs) in microelectronic devices at ground level as do Galactic Cosmic Ray and solar particles in the natural space environment [1]. Radiation Hardness By Design (RHBD) circuit technology developed at UI's NASA Institute of Advanced Microelectronics (IA μ E) have been shown to be effective in 5.0 volt and 3.3 volt CMOS technologies. These RHBD technologies, plus new advancements, have been applied to ULP circuits to mitigate Single Event Effects (SEE). The Total Ionizing Dose immunity of the ULP circuits have been shown to be enhanced over the baseline 0.35 μ m process into a range in excess of 200 krad(Si) [2]. The combination of the ULP and RHBD technologies has been dubbed CMOS Ultra Low Power Radiation Tolerant or CULPRiT.

2. ULP background

The ULP technology represents a combination of an optimized semiconductor foundry process, circuit design, and logic architecture. Traditional approaches to CMOS design assume that static leakage currents should always be minimized. From a practical standpoint, this approach is most applicable to static circuits that are doing no work. The key to the ULP approach is to reduce total energy consumed by *balancing* dynamic power and static power [3]. In deep submicron CMOS technologies, where short channel effects dominate the transistor operating characteristics, the switching speed of a transistor is proportional to the ratio of the operating voltage to the transistor threshold voltage (V_{dd}/V_{th}), but is a very weak function of the actual magnitude of V_{dd} [4]. Aggressively scaling the threshold voltage of active circuit transistors thus allows the circuit to maintain a high level of performance even while the operating voltage is reduced to 500mV or less.

Low tunable thresholds and high speed transistors are obtained by selecting the right substrate doping levels while at the same time optimizing device structures to control punch through. The ULP process has been instantiated around the 0.35 μ m CMOS baseline process at AMI Semiconductor, in Pocatello, Idaho. The unique ULP circuit design comes to play in controlling the tunable thresholds and accounting for the increased static current in inactive circuit sections. The minimum energy and the minimum product of energy * time (speed) are both related to the optimum operating voltage, which is in turn related to the optimum threshold voltage, which is a function of both circuit activity and logic depth. Controlling circuit activity and logic depth are design architecture issues. The ULP program has also included development of the sub-circuits necessary to interface the ULP circuits with conventional technology devices.

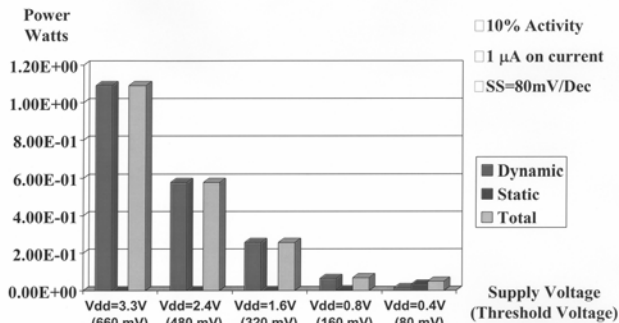


Figure 1. Constant performance power vs. voltage for one million transistor design.

Figure 1 shows a bar diagram of dynamic power, static power, and total power for a hypothetical one million transistor design at constant performance for various combinations of operating and threshold voltage. As a more concrete example, a Reed Solomon telemetry channel coder [5] originally developed for space applications by the IA μ E utilizing the Aeroflex/UTMC 5.0V radiation hardened UTE-R process [6] typically consumes about 880 mW at 200 Mbps. A CULPRiT version of the same functional design operates at a core power of 1.7 mW at 200 Mbps. When driving a 120pF I/O load at 3.3V signal levels, the I/O power alone is 160 mW, which highlights the potential value of complete ULP systems or subsystems over discrete ULP components within a non ULP system. The 200 Mbps is the maximum operating speed for the Aeroflex/UTMC design. The CULPRiT design operates to at least 480 Mbps.

3. SEE hardness by design

Multiple strategies have been applied to harden microcircuits against the effects of SEU. Some design approaches seek to raise the critical charge required to

upset sensitive storage nodes. Various redundancy-based techniques seek to maintain a source of uncorrupted data even after an SEU occurrence and use that data and feedback to recover the upset. Increasing concern must also be paid to the effects of SET in combinational logic. The primary goal of SEU HBD is to produce SEU immune circuits using standard CMOS processing, with no additional mask or processing steps, while minimizing cell size increase, circuit speed loss, and increased power consumption.

3.1. New memory cell design

The enhanced critical charge hardening techniques include increasing transistor drive, capacitive hardening, and resistive hardening. A high drive transistor can quickly remove/replace SEU injected charge, shortening the time duration of the disturbance. Large high drive transistors also have increased node capacitance, which reduce the voltage excursions caused by the SEU injected charge. Increasing the capacitance of critical nodes to reduce the voltage change due to SEU injected charge is the basic concept behind capacitive hardening of circuits and may be used quite effectively for some circuit aspects such as global clocks and other signals such as system resets. Resistive hardening involves the use of resistors in the memory element feedback paths to create, in conjunction with the gate capacitance, a low pass filter to reject the effects of SEU induced transients while passing the longer duration legitimate signals. Outside of the realm of the global signals described above, the enhanced critical charge methods all have adverse impacts on circuit speed and/or power consumption that are outside of the goals of the CULPRiT program.

The first reported redundant design hardened CMOS latch, proposed by Rockett, [7], took advantage of the physics of SEE charge collection by including redundant storage nodes that were driven by, and only connected to, p+ diffusions regions. This meant that if these nodes were struck by an ionizing particle the data stored on the nodes could only be corrupted by a low voltage (zero) upsetting to a high voltage (one), but in the absence of any n+ diffusion, a one would never upset to a zero. Thus, these redundant storage nodes were the source of incorruptible ones. The Rockett design took advantage of this fact and through appropriate transistor sizing was designed such that conflicts that would occur in the memory cell feedback as the result of a particle strike changing one of the nodes would always be resolved in a manner that would correctly recover the upset storage node value.

Following Rockett, the memory cell design proposed

by Whitaker [8,9,10] utilizes similar fundamental concepts of redundant storage nodes holding incorruptible data, with feedback to correct any upset data, and “intelligence” in the feedback based in part on the physically possible direction of charge collection across p-n and n-p junctions. However, instead of effectively adding storage nodes and feedback to the standard six-transistor cell and loading the clock to turn all of the added circuitry off while data is written to the cell and also to drive “data” to one of the redundant nodes during data storage as the Rockett cell did, the Whitaker cell represented a completely new approach. The low power Whitaker cell, shown in Figure 2 with the access and buffer transistors omitted for simplicity, consists of two loadable storage structures. The lower storage structure is a modified six-transistor cell containing only n-channel devices connected to the storage node and the top structure is a modified six-transistor cell containing only p-channel devices connected to the storage node. Transistors M5-M8 are included to completely shut off the off state currents.

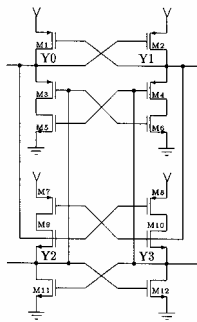


Figure 2. Whitaker SEU immune memory cell

The Whitaker cell has proven to be very successful and has been utilized both in full custom microcircuits for space applications [11] and as the memory cell basis for a radiation tolerant standard cell library [12]. However, the reduced voltage swing at cell interior storage nodes due to p-channel pull down transistors M3 and M4 at Y0 and Y1 and n-channel pull up transistors M9 and M10 at Y2 and Y3 became problematic to the performance of the cell at the aggressively scaled CULPRiT operating voltage.

A formal design synthesis and analysis technique based on the theory of asynchronous sequential circuits has been developed [13] at the IA μ E and used to create a new Single Event Resistant Topology (SERT) cell design [14]. The SERT cell, shown in Figure 3, again with access and buffer transistors omitted for simplicity, utilizes fully complementary p-channel pull-ups and n-channel pull-downs for all nodes. Unlike the Rockett and Whitaker designs, the SERT cell is conflict free during SEU recovery.

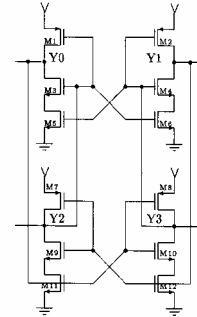


Figure 3. SERT SEU immune memory cell

That is, when a particle strike causes an upset of one storage node the SERT cell feedback is designed to allow nodes to enter a high impedance or tri-state mode, but in no case will one of the storage nodes be pulled up and be pulled down simultaneously. This design feature decreases the power consumption of the cell during SEU recovery and also means that the SEU recovery is never dependent on the relative strength of transistors. This makes the transistor sizing effort much easier at design time. Following the concepts from the theory of asynchronous sequential circuits and considering that each circuit node represents one state variable, the SERT cell design does allow for Multiple Transition Time (MTT) recovery. By contrast, the hardened cell patented by both Barry [15] and Dooley [16] is a Single Transition Time (STT) design. A STT design can recover some hundreds of picoseconds faster than a MTT design, but a MTT design requires fewer transistors. As with the Whitaker cell, the output buffer can be designed such that the cell has fault tolerant output and does not propagate an upset outside of the cell during the SEU recovery time. The cell is also designed to have fault tolerant inputs that do not allow a single input fault to propagate to the internal state variables. This feature is utilized for prevention of SETs that may occur in the combinational logic from being captured into the memory coincident with clock edges.

3.2. Single event transient mitigation

During the early years of RHBD research there was little real concern for SET in combinational logic even if there was academic interest [17]. In the absence of the regenerative feedback found in memory cells the intrinsic signal propagation delay through combinational logic gates would tend to swallow the relatively short duration SET voltage disturbances. The rate of upsets occurring internal to memory cells is essentially independent of the rate at which the memory cells are clocked. For SET capture into memory elements coincident with the clock edges however, the observed error rate should increase linearly with the clock frequency. As modern CMOS processes became faster and faster concern arose that the SET disturbance duration would more and more match

that of real signals being passed by logic circuits. Such a predicted linear error rate increase with clock frequency was observed in 1998 during SEU testing at the Single Event Upset Test Facility (SEUTF) at Brookhaven National Laboratories, confirming the occurrence of a SET becoming a SEU [18]. The tested chips were fabricated in both 0.5 μm and 0.35 μm technologies and SET upsets were observed in each chip in circuit sections that were designed in a “gate array” style where all transistors are similarly sized. Other sections of the same test chips incorporated circuit design techniques where transistors were carefully sized to match signal rise and fall times, which reduces the spreading of transient glitches. These sections also incorporated a temporal separation scheme for providing the two input signals to the dual input fault tolerant SEU immune flip-flops such that an SET is not presented to both inputs simultaneously [19,20]. Testing demonstrated these design techniques to be effective in eliminating the observed SET upsets. These same SET mitigation techniques have been utilized in the CULPRiT device designs.

3.3. Single event latchup mitigation

The use of p+ guard bars around the n-channel transistors and n+ guard bars around the p-channel transistors [21] has been shown to be very effective in the elimination of Single Event Latchup (SEL) in CMOS microcircuits, even when the use of an epi starting material is not completely effective [18]. Guard bars are produced during the normal source/drain mask steps and require no special processing. The cost in cell area for the inclusion of p+ and n+ guard bars is typically 10-15%. Various devices fabricated using many different CMOS processes have consistently shown no SEL in guard bar protected circuits up to the highest LET tested (LET > 90 MeV-cm²/mg). Even though the 500 mV operating voltage is expected to be lower than the voltage that would be required to sustain a latchup condition, because of the presence of the higher back bias voltages the guard bars have been included in all of the CULPRiT devices designed and tested to date.

3.4. CULPRiT SEE test results

The CULPRiT technology Reed Solomon telemetry channel coder [22] was tested by the NASA Goddard Space Flight Center Radiation Effects Group personnel, June 27-28, 2002 at the SEUTF at Brookhaven National Laboratories. The SEU onset and saturation cross-section data are shown in Figure 4. The onset threshold is about 20 MeV-cm²/mg and the saturation cross-section is about 17 μm^2 /bit. No SEL was observed up to the maximum effective LET test value of 90 MeV-cm²/mg.

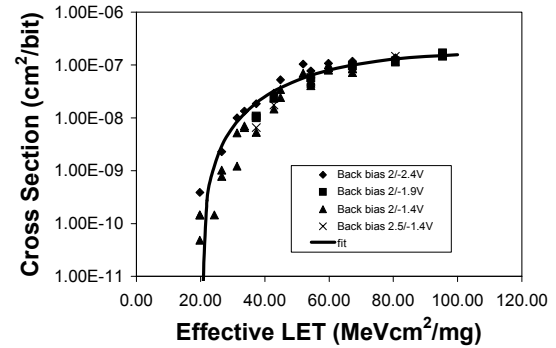


Figure 4. Reed Solomon encoder SEU test results

A SEU threshold of 20 MeV-cm²/mg is sufficiently high to eliminate concerns for proton induced upsets leaving only GCR concerns. Analysis of this and other test results are continuing. It is believed that the observed SEU threshold may be the result of a close proximity of co-sensitive nodes in the cell layouts used and that these SEU results can be further improved in the future.

4. Total ionizing dose

TID radiation tests of ULP circuits utilizing back bias design techniques to electrically alter the native transistor thresholds have produced very promising results up to the test limit of 200 krad(Si) [2]. The reduced voltage that is applied to the circuit during operation increases the recombination chances for ionized electron/hole pairs and thus reduces the yield of radiation generated holes trapped in the oxides. Additionally the application of back bias increases (via body effect) the threshold of the parasitic n-channel transistors in the field and edge regions, which further reduces the flow of parasitic leakage currents. Figure 5, taken from reference [2] shows the effect of the application of back bias on transistor leakage current after exposure to a dose of 200 krad(Si). Although testing has not yet been conducted to higher dose levels, based on results to date, it is believed that such circuits could easily be TID hard up to 1 Mrad(Si) and beyond.

5. CULPRiT devices

The Reed Solomon telemetry channel coder device is being qualified for space flight by PicoDyne Corporation for the New Millennium Program ST5 mission. Other CULPRiT devices that have been designed and produced include a C50 DSP [23], a CCSDS Lossless Data Compressor [24], a Reed Solomon encoder/decoder for Solid State Recorder applications, a 8051 microcontroller, and a high speed correlator [25]. The 8051 and Lossless Data Compressor (USES) are scheduled to be radiation tested during the coming months and the 8051 will be included as a part of a NASA Electronic Parts and

Packaging Program (NEPP) study to evaluate several radiation mitigative approaches [26].

6. Acknowledgements

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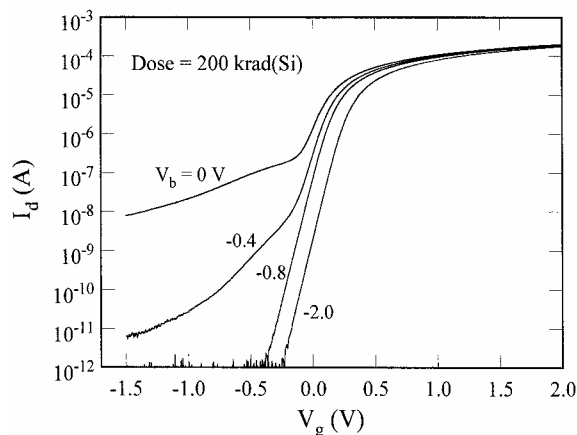


Figure 5. Effect of back bias on TID induced leakage

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