

An Ultra-Low Power, Radiation Tolerant, High Speed Correlator¹

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Abstract

A digital high-speed cross-correlator (HSCC) has been developed for use in a microwave polarimetry instrument. The HSCC incorporates radiation tolerant circuit design and an ultra-low power CMOS process. In order to meet the very high input data requirement of 500 megasamples per second the correlator architecture was partitioned into different sections, each with its own trade-off requirements for the maximum operating frequency and degree of radiation tolerance. An ultra-low power, radiation tolerant, standard cell library was created to allow commercial design tools and methods to be used for the integrated circuit design. These tools made it possible to synthesize the gate-level circuits from behavioral models and also to automatically generate layouts for circuit modules. Level-shifting interface circuits were developed to allow the correlator to communicate with conventional digital circuits using a 3.3 volt power supply while the correlator core operated with a supply voltage of 0.5 volts. Preliminary test results indicate that the correlator functions properly for clock frequencies of several hundred megahertz with milliwatts of power consumption.

1. Introduction

Understanding the Earth's climate is one of the primary science missions undertaken by NASA, and information regarding the wind vector at the ocean's surface is a vital part of that understanding. Measurements of ocean wind speed and direction are necessary to develop a complete comprehension of the variability of our climate, which in turn enables more accurate weather prediction.

Passive microwave polarimetry has demonstrated a capability for measuring wind speed and direction at the surface of the ocean. Furthermore, NASA has identified microwave polarimetry as an enabling technology for future remote sensing missions [1]. The practical application of microwave polarimetry requires the computation of the cross correlation between the horizontally and vertically polarized components of the received microwave energy. Furthermore, for instruments on board spacecraft it is very important that

power consumption is minimized and that the electronic systems can tolerate the natural radiation environment of an earth orbit.

The goal of this development effort was to deliver a digital cross correlator circuit that could operate at very high data rates while consuming little power and maintaining a high degree of radiation tolerance.

2. Cross correlator function

A simple block diagram for the passive microwave polarimeter is shown in Figure 1. The two sensors shown in this figure represent the horizontal and vertical polarization components from a dual-polarization radiometer. The IF section of the instrument performs quadrature demodulation, and the analog-to-digital converters (ADCs) digitize the resulting signals at a rate of 500 Msample/second.

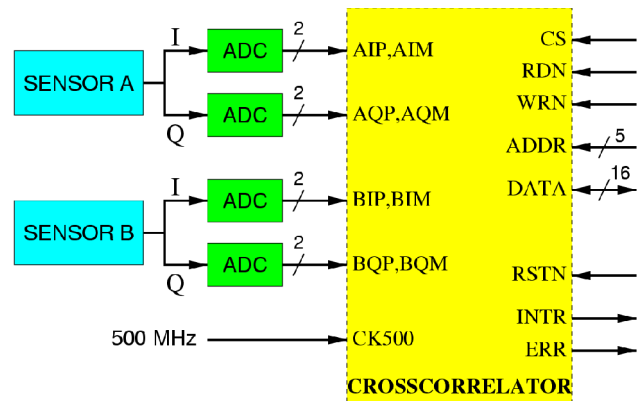


Figure 1. Polarimeter block diagram

The high-speed cross correlator is used to determine the degree of correlation between the in-phase and quadrature components of two signals. The four signal inputs accommodate digitization to three levels (-1, 0, +1). The inputs are sampled at up to 500 MHz and the correlation count is integrated for up to 2^{24} clock cycles. The integration time is programmable with a step size of 2^8 clock cycles.

The correlator is designed for use with a microprocessor and supports a simple bus-oriented interface. At the end of the integration time an interrupt signal will be asserted to indicate that new correlation

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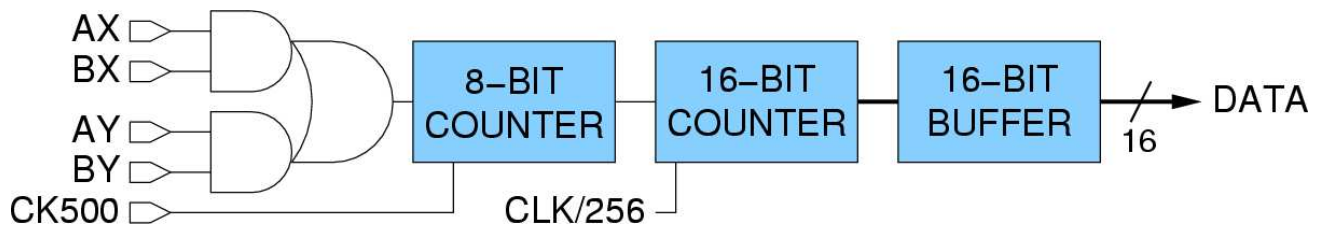


Figure 2. Correlation slice

data is available. The microprocessor then reads the data from the device, supplying a 5-bit address to select the data of interest. The data values are buffered so that a new integration cycle can occur while data from the previous cycle is read.

For purposes of discussion we will refer to the two incoming data streams as A and B. Each data stream consists of both an in-phase and a quadrature component, which are designated with I and Q. Finally, these signals are digitized to three levels. Two bits are required to represent these three levels and they are called P for plus and M for minus. For example, the two input bits for the quadrature component of data stream A are AQP and AQM. When AQP is a logic '1' and AQM is a logic '0' the quadrature component of stream A has the integer value +1. When AQP is '0' and AQM is '1' the integer value is -1, and when both AQP and AQM are '0' the integer value is 0.

The basic functionality of the correlator is embodied in sixteen *correlation slices*. Each slice contains identical logic, as shown in Figure 2. The first section of the correlation slice is the logic gate that computes the desired correlation of the A and B inputs, shown generically as AX, AY, BX and BY. For example, one slice will be used to compute the direct (positive) correlation between the quadrature components of A and B, which is denoted as QQ+. In this case AX will be connected to the AQP input and BX will be connected to the BQP input while AY will be connected to the AQM input and BY will be connected to the BQM input. Similarly, to compute IQ-, the inverse (negative) correlation between the in-phase component of A and the quadrature component of B, a correlation slice is used with AX connected to AIP, BX connected to BQM, AY connected to AIM, and BY connected to BQP.

The logic gate output is sampled by the input CLK signal, and an 8-bit counter increments in every clock cycle when the logic gate output is asserted. Thus, the most significant bit of the counter will have a frequency equal to the frequency of the logic gate output signal divided by 256, when observed over relatively long periods of time.

The most significant bit of the 8-bit counter is then sampled by a 16-bit counter. The 16-bit counter uses a clock derived from the CLK input and is incremented every time (within 256 CLK cycles) that the 8-bit counter rolls over. When the desired integration time is reached the contents of the 16-bit counter are copied to a buffer,

and the 16-bit counter is cleared to begin a new accumulation cycle.

At the end of the integration time period an interrupt signal, INTR, is asserted to indicate that new data is available in the correlation slice buffers. If the buffers are not read before the end of the next integration time period then the data for the previous integration time will be lost and the error signal, ERR, will be asserted.

Figure 3 shows a block diagram of the entire correlator chip. Eight correlation slices are used to compute all of the direct and inverse cross correlations between the two input channels, and eight additional slices are used to simply count the occurrence of '1' states on the eight data input pins.

The correlator has a simple interface to a host microprocessor and functions much like a small random-access memory (RAM) containing 32 16-bit words. Level shifting circuits are used in this interface, which operates at standard 3.3V logic levels [8]. The microprocessor controls the function of the correlator and sets the desired integration time by writing appropriate values to registers in the correlator. The correlation slice accumulator buffers can be read as a sequential group of memory locations.

3. Ultra low power CMOS technology

The primary motivation for the development of the HSCC was to significantly reduce the power consumption of the polarimeter. A breadboard prototype of the correlator using ECL logic consumed approximately 20W, which was felt to be excessive for a spacecraft application.

Simulations suggested that the ultra low power (ULP) CMOS technology could easily reduce the correlator power consumption by at least an order of magnitude. ULP CMOS achieves dramatic reductions in power consumption by reducing the power supply voltage to just 500mV [2,3]. Since the dynamic power consumption of a CMOS circuit is proportional to the square of the supply voltage, small changes in supply voltage can achieve large power savings [4,5]. However, at very low operating voltages the normal variation in transistor threshold voltages, as a result of manufacturing tolerances and environmental factors, can make it difficult to design robust circuits[9]. To compensate for these variations the ULP technology employs a back bias

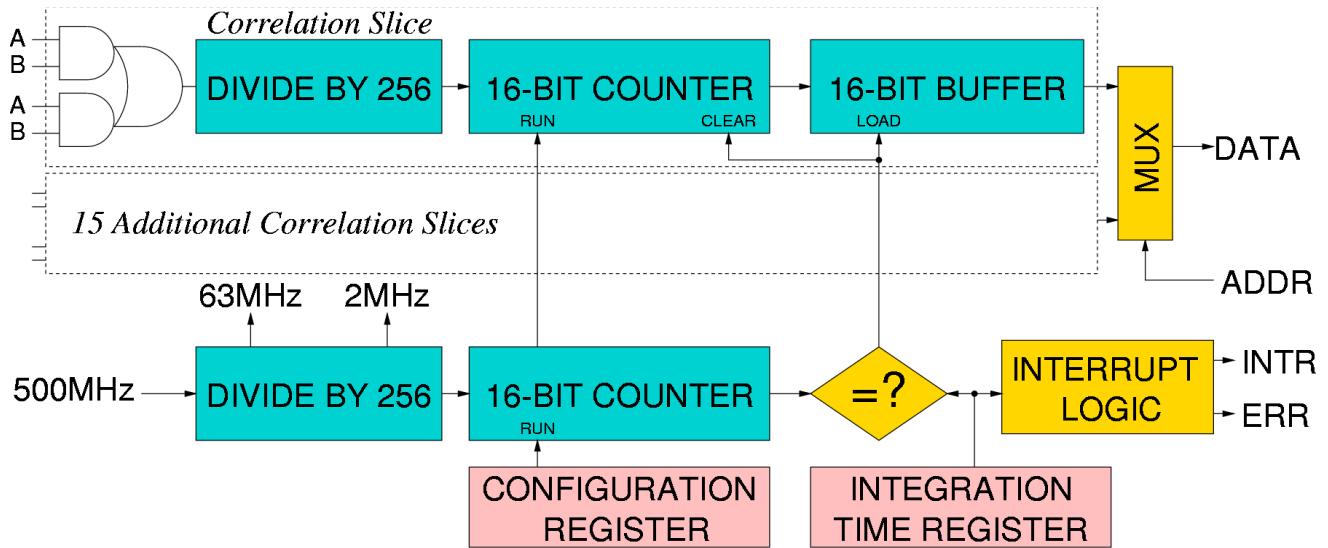


Figure 3. Correlator chip block diagram

scheme that allows the transistor threshold voltages to be tuned for each environment and application.

4. RT ULP design issues

Achieving radiation tolerance at a supply voltage of 500mV presents new challenges [10]. Total ionizing dose degradation and single event latchup do not appear to be serious threats for ULP CMOS, but providing resistance to single event upset (SEU) is much more difficult. At first glance it would appear that traditional design techniques for SEU mitigation simply can not be applied to a device operating at a clock frequency of 500MHz so a unique strategy was developed in order to achieve the goals of high operating frequency and radiation tolerance.

The correlation slice was divided into three stages and different radiation hardness by design (RHBD) techniques were applied to each stage. The first stage includes the logic gate that performs the signal multiplication and a divide-by-16 prescaler, all operating at 500MHz. The second stage provides a second divide-by-16 prescaler clocked at 63MHz. The third stage operates at just 2MHz and contains the 16-bit counter and buffer register.

For 500MHz operation it was also necessary to design custom data and clock input pads, as shown in Figure 4. The input pads serve to synchronize incoming data to the internal clock, and adjust the relative delays between the clock and data signals. The 500MHz flip flops use both true and inverted clock signals and any skew between these signals increases the effective delay through the flip flop. Two pairs of 500MHz clock signals are used. The first pair, CKP and CKPN, is distributed along the pad ring to the data input pads while the second pair, CKI and CKIN, is the internal clock that drives the first stage of

each correlation slice. In both cases the delay through the buffer that drives the true clock has been carefully adjusted to match the delay through the inverter that drives the inverted clock. In addition, the internal clock is further delayed to compensate for the delay through the flip flop in the data input pad, leaving the maximum time for the correlation logic.

The first stage of the correlation slice, shown in Figure 5, computes the correlation (multiplication) function using a single AND-OR-2-2 gate. The first flip flop toggles at the rising edge of CK500 if the output of this gate is high. The next three flip flops in this stage are arranged as a ripple counter, which can operate at much higher frequencies than a parallel synchronous counter.

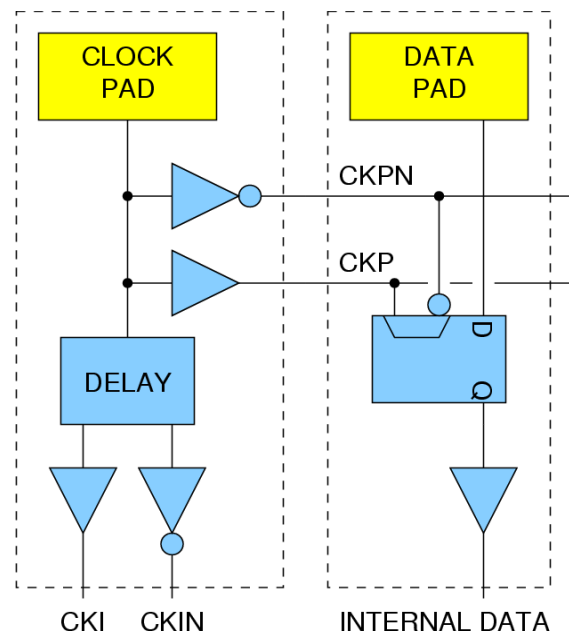


Figure 4. Custom input pads

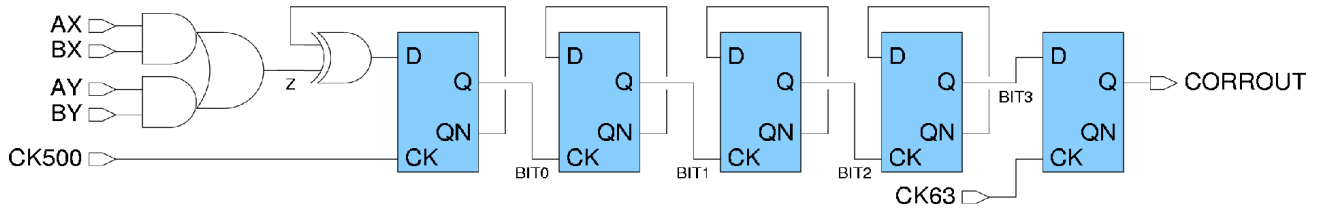


Figure 5. Stage 1 of correlation slice

However, the total delay through this ripple counter can be longer than the incoming clock period. The final flip flop in this stage resynchronizes the counter output to the 63MHz system clock.

Full-custom design techniques were used for the first stage because of the very high clock speed that was required. Parasitic capacitances and RC delays are matched for each of the slices for uniform behavior. Because of the need for extremely high circuit speed the 500MHz first stage counter does not use SEU-immune flip flops. However, these circuits use large transistors to achieve high performance and should show reasonably good SEU behavior for non-hardened circuits. Since transient errors in the first stage cause an error of no more than one-sixteenth of an LSB in the output this was deemed to be an acceptable compromise between circuit performance and radiation tolerance.

The counters in the second stage were synthesized from a behavioral VHDL description, using Synopsys tools. The target technology for the synthesis is an RT ULP standard cell library developed at CAMBR. Synthesis constraints were applied to insure that the final netlist met all speed requirements and had sufficient output drive. The 63MHz second stage sections use SEU tolerant flip flops but do not include design features to reduce SEU from hits to the combinational logic, known as Single Event Transients (SET). However, additional synthesis constraints were used to limit the maximum transition time of the output node of each gate, which helps to reduce the threat of SET by also limiting the maximum recovery time from a cosmic particle strike. Note that an SEU in the second stage causes an error of no more than 1 LSB in the output.

The low speed circuits in the third stage sections were also synthesized from a behavioral VHDL description. The 2MHz sections of the correlation slice and clock counter use SEU-tolerant SERT flip flops with temporal

separation, which has been shown to reduce the number of errors from SET in earlier, non-ULP, circuits [6, 7, 11]. Temporal separation, rather than full dual rail logic, was selected for two reasons. First, the low clock frequency in the third stage reduces the probability of an SET being latched as an SEU. Second, using dual rail logic in the third stage sections would greatly increase the number of transistors, and therefore the leakage current, in the design.

The I/O control section implements the asynchronous interface to the host microprocessor or data acquisition interface. It was specified in behavioral VHDL and synthesized to a dual-rail configuration for maximum resistance to SEU. Dual-rail logic takes advantage of the inherent redundancy in the RT flip flops and extends that redundancy into the combinational logic as well. The RT flip flop [12] can be configured with two separate inputs, such that the state of the flip flop will not change unless both inputs have the same logic value. The two flip flop inputs are then driven by two identical but distinct blocks of combinational logic. Therefore, an SET occurring in either of the two combinational blocks will not cause the flip flop to enter an incorrect state. One disadvantage of the dual-rail technique is that the clock period must be extended to allow time for either of the combinational blocks to recover from an SET and return to the correct state. Of course, dual-rail logic also requires nearly twice the area and power.

Applying dual-rail techniques to the I/O control section is appropriate for several reasons. First, the function of this section of the design is most critical and errors in the control logic could cause a serious loss of data. Second, the operating frequency of the control logic is quite low, allowing ample time for SET recovery. Finally, the area and power consumed by the control logic is a small fraction of the total so there is little penalty in doubling the size of the combinational logic.

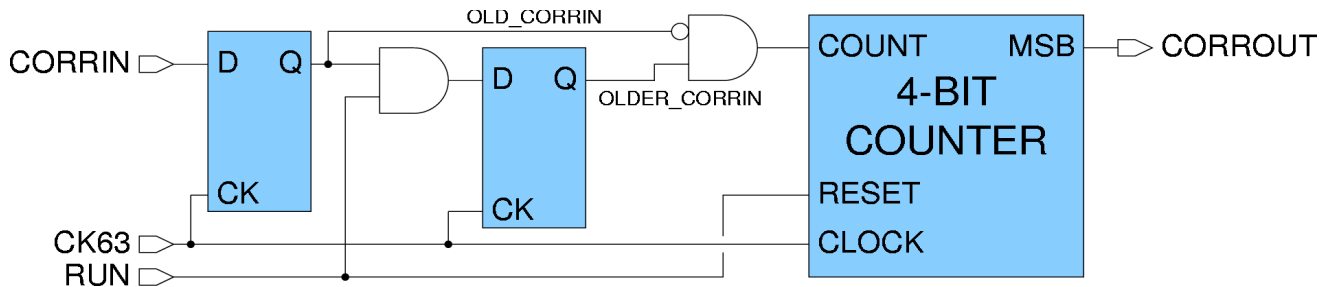


Figure 6. Stage 2 of correlation slice

Commercial integrated circuit design tools typically seek to eliminate redundancy so it was necessary to modify the conventional standard cell design flow in order to implement dual-rail logic. Within the synthesis tool we used scripts that automatically separated the combinational logic from the flip flops, replaced the conventional single-rail flip flops with our dual-rail flip flop, duplicated the combinational logic block and then correctly rewired the connections between the logic and flip flop blocks. The automatic layout tools were constrained to produce the blocks of flip flops and logic so that they could be connected by abutment, with the flip flops in the center and one logic block on each side. This arrangement has the added benefit of providing a physical separation between the logic blocks and making it impossible for one cosmic particle to affect the logic state of both blocks.

5. Conclusions

A high speed cross correlator ASIC was developed for use in microwave polarimetry instruments. It supports input data rates of several hundred megahertz while consuming a small fraction of the power used by previous correlators. In order to support the requirements of high performance and radiation tolerance, the design was partitioned into several sections. Different techniques were used in each section to achieve hardness-by-design. These techniques are compatible with commercial ASIC design tools and methods. Preliminary testing indicates that the correlator is functional at clock frequencies up to 500MHz with a power consumption of less than 10mW.

6. References

[1] J. Piepmeier and J. Hass, "Ultra-low Power Digital Correlator for Passive Microwave Polarimetry", *Earth Sciences Technology Conference*, August 30, 2001.

[2] J. Burr and A. M. Peterson, "Ultra low power CMOS technology", *NASA Symposium on VLSI Design*, October 1991, pp. 4.1.1-4.1.10.

[3] J. Burr, "Stanford Ultra Low Power CMOS", *IEEE Low Power Workshop*, August 1993.

[4] R. Gonzalez, B. M. Gordon and M. A. Horowitz, "Supply and threshold voltage scaling for low power CMOS", *IEEE Journal of Solid State Circuits*, August 1997, pp. 1210-1216.

[5] D. Liu and C. Svensson, "Trading speed for low power by choice of supply and threshold voltages". *IEEE Journal of Solid State Circuits*", pp.10-17, January 1993.

[6] K. J. Hass, J. W. Gambles, B. Walker and M. Zampaglione, "Mitigating Single Event Upsets from Combinational Logic", *7th NASA Symposium on VLSI Design*, October 1998, pp. 4.1.1-4.1.10.

[7] K. J. Hass and J. W. Gambles, "Single Event Transients in Deep Submicron CMOS", *42nd Midwest Symposium on Circuits and Systems*, August 1999.

[8] K. J. Hass and D. F. Cox, "Level Shifting Interfaces for Low Voltage Logic", *9th NASA Symposium on VLSI Design*, November 2000, pp. 3.1.1-3.1.7.

[9] K. J. Hass, J. Venbrux and P. Bhatia, "Logic Design Considerations for 0.5-Volt CMOS", *2001 Conference on Advanced Research in VLSI*, March 14-16, 2001, pp. 75-85.

[10] J. W. Gambles, K. J. Hass and S. R. Whitaker, "Radiation Hardness of Ultra Low Power CMOS VLSI", *11th NASA Symposium on VLSI Design*, May 2003.

[11] J. W. Gambles, K. J. Hass and K. B. Cameron, "Apparatus For and Method Of Eliminating Single Event Upsets In Combinational Logic", U.S. Patent No. 6,326,809, December 4, 2001.

[12] G. K. Maki, K. J. Hass, Q. Shi and J. Murguia, "Conflict Free Radiation Tolerant Storage Cell", U.S. Patent Application Serial No. 09/776,453, February 2, 2001.