

Design of a CMOS Low Noise Amplifier (LNA) at 5.8 GHz and Its Sensitivity Analysis

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Abstract

This paper presents a 5.8 GHz low voltage and low power LNA design integrated in a TSMC 0.18 μm CMOS process, and its sensitivity analysis. This sensitivity analysis gives a measure of the sensitivity of the LNA performance to a change in the circuit element values, thereby assisting the designer choose the adequate circuit-element tolerances. Such sensitivity analysis of the LNA is very beneficial for making appropriate design trade offs. The designed LNA requires only a 1 V supply voltage and consumes 4.5 mW DC power. At 5.8 GHz, this LNA has noise figure (NF) of 2.463 dB, with input return loss of -15.35 dB, output return loss of -16.26 dB, and voltage gain of 11.57 dB.

1. Introduction

The first stage of a receiver is typically a low noise amplifier (LNA), whose main function is to provide enough gain to overcome the noise of subsequent stages (such as mixer) [2]. In the literature, there are many LNA work designed in GaAs and bipolar technology [3, 7]. As the cutoff frequency of CMOS device has increased above a few tens of GHz, CMOS circuits are capable of replacing GaAs/bipolar circuits in the area of a few-GHz RF. Since CMOS technology has the feature of low cost, high level of integration, and mass productivity, it becomes very popular in RF integrated circuit design currently [4].

Many research have been done in CMOS LNA area from 900 MHz to 2.4 GHz [8, 1, 5, 2, 6]. As the demand for Radio Frequency Integrated Circuit's operating at higher frequency bands increases, circuit design in an IEEE 802.11a standard becomes a very interesting area. However, there are fewer examples of CMOS LNA designed at 5-6 GHz.

In this paper, a low voltage and low power CMOS LNA at 5.8GHz is proposed. As a design tool, sensitivity anal-

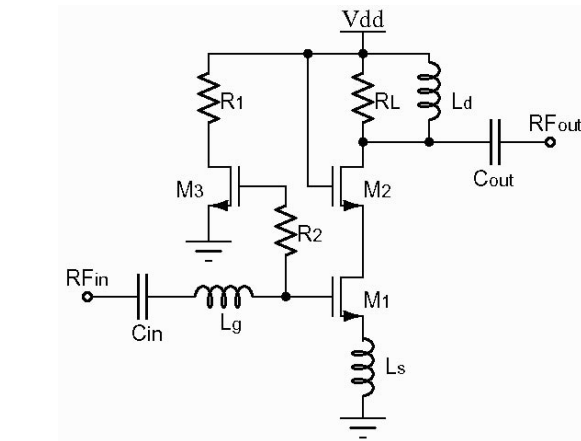


Figure 1. Complete schematic of the 5.8GHz LNA

ysis gives a measure of sensitivity of the LNA circuit performance to a change in the circuit element values, thereby assisting the designer in choosing adequate circuit-element tolerances. Such sensitivity analysis of the LNA is very beneficial for making appropriate design trade offs. In this paper, the sensitivity analysis of the proposed LNA circuit is also provided.

The remainder of this paper is organized as follows: In the next section, a single-ended 5.8 GHz RF CMOS LNA circuit design is proposed. Section 3 shows the simulation results. Section 4 describes the sensitivity analysis of the proposed LNA design. Finally, some conclusions are given in Section 5.

2. LNA Circuit Design

The complete schematic of the 5.8 GHz LNA is shown in Figure 1, where L_g , L_s , and L_d are all implemented with

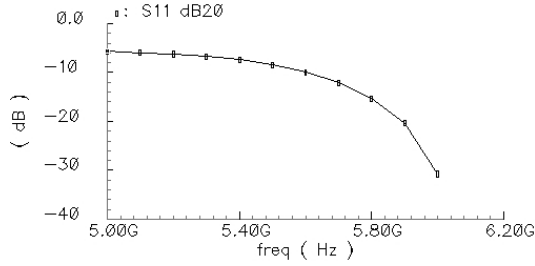


Figure 2. LNA s11

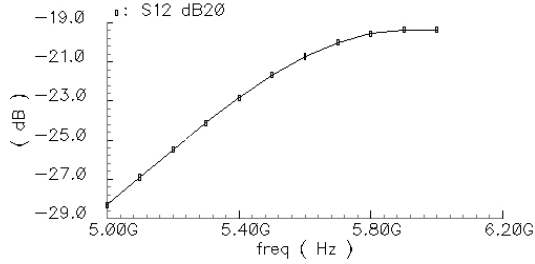


Figure 3. LNA s12

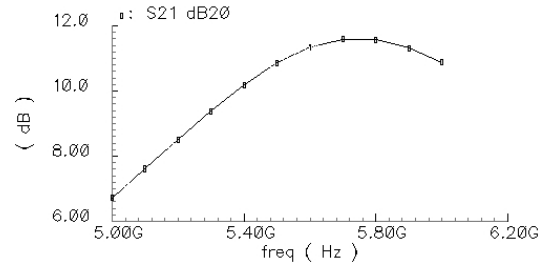


Figure 4. LNA s21

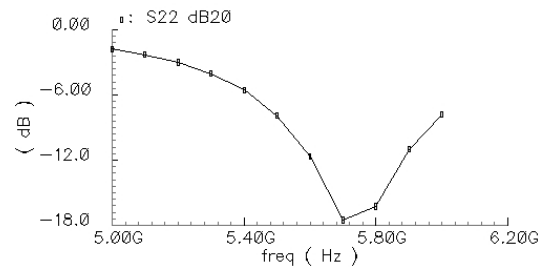


Figure 5. LNA s22

on-chip spiral inductors. The method employed here is inductive source degeneration. Cascoding transistor M_2 is used to reduce the interaction of the tuned output with the tuned input, and to reduce the effect of the gate-drain capacitance C_{gd} of M_1 . The inductors L_g and L_s are chosen to provide the desired input resistance, L_d and the capacitance of the transistors M_2 form a tank circuit to tune the LNA to 5.8GHz. M_3 , R_1 , and R_2 form a bias circuit. Transistor M_3 essentially forms a current mirror with M_1 , where its width is a small fraction of the width of M_1 's in order to minimize the power overhead of the bias circuit. C_{in} and C_{out} are DC blocking capacitors.

Due to the limited choice of inductor and capacitor values in the technology we choose, the matching network becomes very challenging. With the comprehensive consideration of the chip size and different performance trade-off, C_{in} and C_{out} play important roles in input and output matching respectively. The load resistor R_L is tuned to manage the tradeoff between gain, output matching, and power dissipation of LNA. Both input and output are matched to 50 Ω .

3. Simulation Results

For the proposed single-ended LNA shown in Figure 1, the simulation result is shown in Figure 2–Figure 7. The designed LNA requires only a 1 V supply voltage and consumes 4.5 mW power. At 5.8 GHz, this LNA has noise figure (NF) of 2.463 dB, with input return loss of -15.35 dB, output return loss of -16.26 dB, and voltage gain of

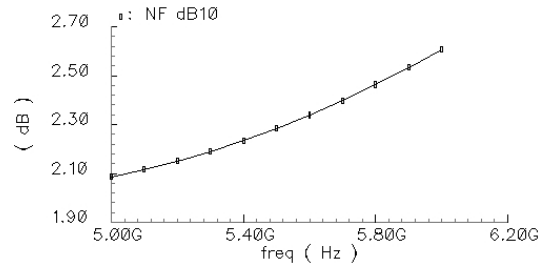


Figure 6. LNA Noise Figure

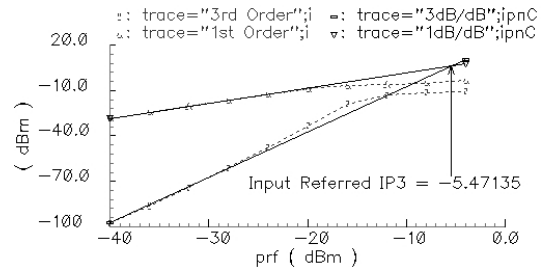


Figure 7. LNA IIP3

Table 1. Performance Summary of LNA

Parameter	Value
Technology	0.18 μm CMOS
Frequency	5.8 GHz
Gain	11.57 dB
NF	2.463 dB
S_{11}	-15.35 dB
S_{22}	-16.26 dB
S_{12}	-19.56 dB
IIP3	-5.47dBm
Supply Voltage	1 V
Power Dissipation	4.5 mW

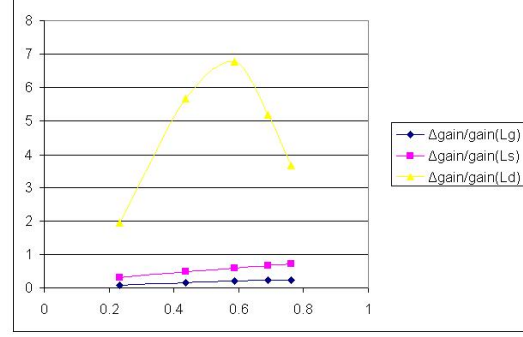


Figure 8. LNA gain variation versus L_g , L_s , and L_d variation

Table 2. comparison to other low voltage CMOS LNA's operation above 5 GHz

	This Work	[9]
Technology	0.18 μm CMOS	
Frequency	5.8 GHz	
Supply Voltage	1 V	
Power Dissipation	4.5 mW	22.2 mW
Gain	11.57 dB	13.2 dB
NF	2.463 dB	2.5 dB
S_{11}	-15.35 dB	-5.3 dB
S_{22}	-16.26 dB	-10.3 dB

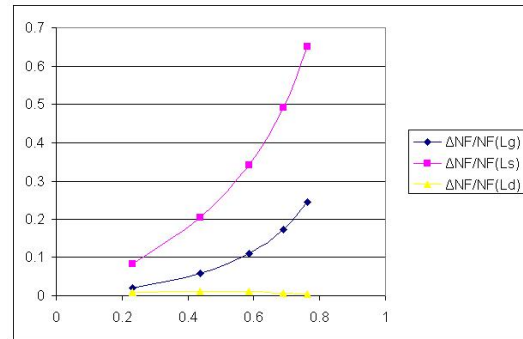


Figure 9. LNA noise figure variation versus L_g , L_s , and L_d variation

11.57 dB. This LNA performance represents high voltage gain, low supply voltage, low noise figure, and low power dissipation. The performance summary is listed in Table 1.

Table 2 lists the comparison to another low voltage CMOS LNA's operation above 5 GHz. Note that [9] represents the experimental results.

4. LNA Sensitivity Analysis

In this section, sensitivity analysis of the proposal LNA is described. We mainly focus on the sensitivity analysis of gain and noise figure to the inductors. Suppose we are interested in the sensitivity of the gain to L_g , L_s , and L_d . We choose the same variation for L_g , L_s , and L_d , then we calculate $\Delta L/L$, and $\Delta\text{gain}/\text{gain}$. Note that gain is in an absolute value, not in dB.

The overall stage transconductance G_m is

$$G_m = g_{m1}Q_{in} = \frac{g_{m1}}{\omega_0 C_{gs}(R_s + \omega_T L_s)} \quad (1)$$

where

$$\omega_0 = \frac{1}{\sqrt{(L_g) + L_s C_{gs}}} \quad (2)$$

The gain of LNA is

$$A_v = G_m Z_L. \quad (3)$$

It shows that the gain is determined by transistor size, L_g , L_s , and load impedance Z_L .

The gain, noise figure, and the third order input intercept point (iip3) variation versus L_g , L_s , and L_d variation are shown in Figure 8–Figure 10.

From Figure 8 and Figure 10, we can see that both the gain and iip3 are more sensitive to the change in L_d compared to L_g and L_s . They also indicate that both the gain and are iip3 are more sensitive to the change in L_s than L_g .

From Figure 9, we can see that the noise figure is more sensitive to the change in L_s and L_g than L_d . And it shows that the noise figure is more sensitive to the change in L_s than L_g .

5. Conclusions

This paper presents a 5.8 GHz LNA design integrated in a TSMC 0.18 μm CMOS process, and its sensitivity anal-

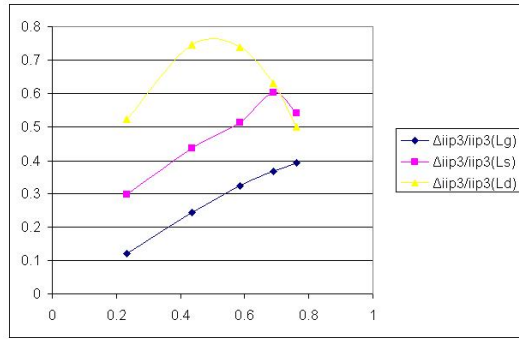


Figure 10. LNA iip3 versus L_g , L_s , and L_d variation

ysis. Such sensitivity analysis of the LNA provides some insights of the proposed LNA design. The designed LNA requires only a 1 V supply voltage and consumes 4.5 mW power. At 5.8 GHz, this LNA has noise figure (NF) of 2.463 dB, with input return loss of -15.35 dB, output return loss of -16.26 dB, and voltage gain of 11.57 dB. This LNA performance represents high voltage gain, low supply voltage, low noise figure, and low power dissipation. This LNA can be used for low voltage and low power wireless applications. Future work may be focused on LNA optimization analysis based on the results of the sensitivity analysis.

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