

# A Family of Analog and Mixed Signal VLSI ASICs for NASA Science Missions

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## Abstract

*Abstract – This paper presents several analog and mixed signal VLSI chips that have been successfully developed over the past several years at JHU/APL for space science missions. The chips have applications on spacecraft avionics and several types of instrumentation. The family of the chips include: the TRIO Smart Sensor multiplexed ADC chip for spacecraft/instrument avionics, the Time of Flight chip for precise time interval measurement, the Energy Chip for low noise particle/photon measurement, a Commandable Discriminator Pulse High Analyzer, Event Accumulator, a radiation hardened voltage reference, an ADC and other. The talk will address some design, radiation hard by design, design for testability, testing, and space qualification issues. The talk will also briefly describe the spacecraft and instrument applications of these chips including: the Cassini mission, Image, Contour, Messenger, Stereo, Pluto, Europa.*

## 1. Introduction

In recent years there is a systematic effort in the space community for spacecraft and instrument miniaturization. In the spacecraft level the traditional “box” based architectures are replaced with modular back-plane architectures [1,2,3,5]. In the instrument level similarly sensors and the electronics are approached with aggressive miniaturization technologies. A key technology in this progress is VLSI microelectronics. In the VLSI approach the designer composes a system-on-a-chip (SoC) based on basic virtual elements, same way a conventional design is based on discrete components. However the difference is obvious since each VLSI element could be by itself a SoC and the overall system much smaller.

The applicability of the VLSI approach in space depends on special design considerations and the fabrication technology. The combined effort should target

high quality, latch-up and SEU immunity, radiation hardness, and other space qualification factors. This approach might require increased initial effort, but as soon as certain key chips are developed the benefit is high [1].

A family of VLSI ASICs has been developed over the years at JHU/APL, tested and space qualified, and now are part of many spacecraft and science instruments. The family of the chips includes among others:

1. The TRIO Smart Sensor for spacecraft/instrument avionics.
2. The Time of Flight (TOF) chip for precise time interval measurement.
3. The Energy chip for the energy measurement of radiation events.
4. Commandable threshold Pulse Height Analyzer.
5. Event Accumulator.
6. Radiation hardened voltage reference.

This paper will briefly present three of the above SoC developments: the TRIO, TOF, and Energy chips.

## 2. The TRIO Smart Sensor Chip for Spacecraft/Instrument Avionics.

Traditionally, a satellite’s electronic circuits have been organized in several subsystems, each housed in its own “black box”. This approach leads to big structures, consisting of multiple boxes interconnected with complex, heavy wire harness. A recent approach in electronics is to replace the boxes with one single, lightweight, composite chassis, housing all the subsystems – communications, guidance, navigation, attitude, power control, health and safety, command and data handling. The architecture is modular and the subsystems communicate through a common backplane, much the same way as the various cards in a PC. This architecture has been termed as the Integrated Electronics Module (IEM) [2,3,,5]. The IEM can be configured to satisfy a wide range of requirements and minimizes development costs while maximizing mission flexibility.

Figure 1 shows IEM block diagram of the JPL X2000 Bus Telemetry Collection Architecture [4]. The

shown in the bottom panel of Figure 2. RIO is a radiation hardened, single chip, multichannel, data acquisition

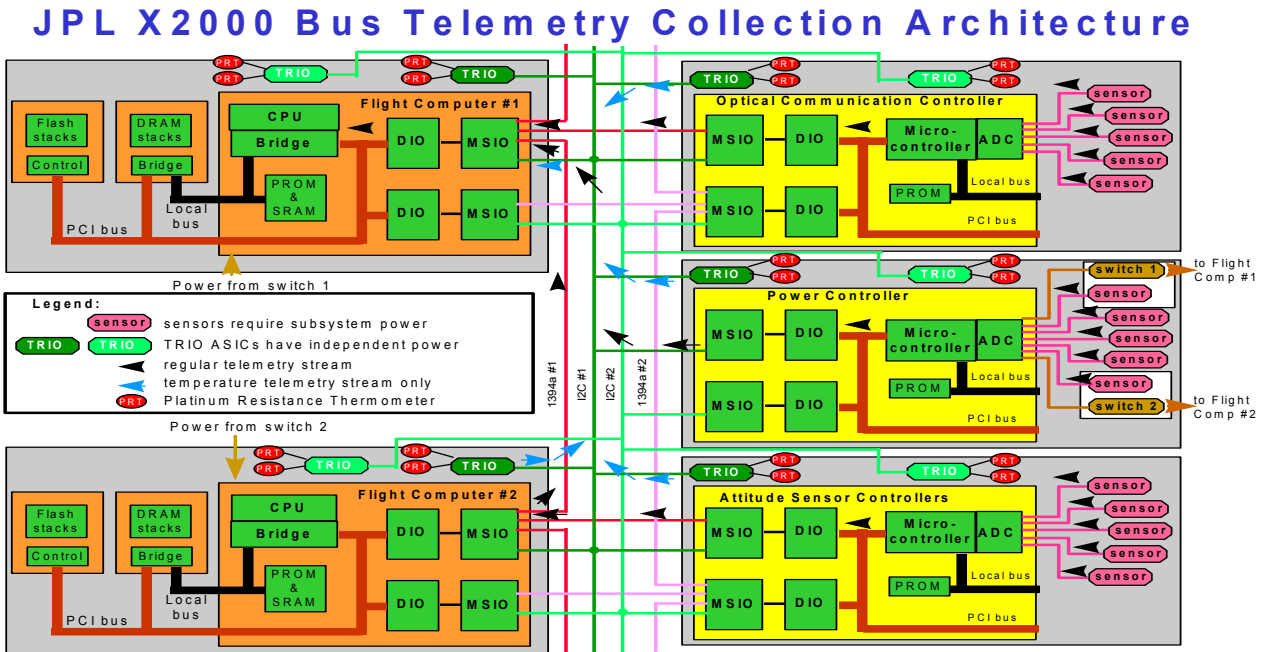


Figure 1. JPL X2000 Spacecraft Bus Telemetry Collection Architecture

X2000 bus is a generic system intended to support NASA's future planetary exploration program. At least five missions are scheduled to use this bus: Europa, Champollion/Deep Space 4, Mars Sample Return, Pluto-Kuiper Express, and Solar Probe. Both APL and JPL, as well as several commercial enterprises, are using similar IEM architectures for their new spacecraft.

The communication of the various subsystems—Flight Computers, Optical Communication Controller, Power Controller, Attitude Sensor Controllers—in the X2000 bus architecture is based on two redundant, industry standard, serial buses: the high-speed IEEE 1394, and the low-speed I2C. The fast bus typically operates at 50-400 Mb/s and is used to communicate spacecraft attitude, science and other housekeeping data. The low speed bus typically operates at 100 or 400 kb/s and is used for spacecraft health and engineering data collection from several distributed sensors. In both cases the serial approach essentially eliminates miles of harnessing compared to the conventional box approach. The enabling microelectronics technologies for this spacecraft design approach are the 1394 bus interface chip and the generic APL Remote Input Output (RIO) chip.

APL's generic RIO chip is a mixed-signal ASIC specifically to enable distributed spacecraft and instrument health data collection through the low-speed I2C bus, as well as local data collection through a standard parallel bus. A block diagram of the RIO is

device that can digitize many types of engineering data and deliver through a serial or a parallel bus. The device in its complete version will measure temperatures, voltages, currents, radiation dose in spacecraft penetrating profiles, and pressure. The sensing capability can extend to any other physical quantity that can be transduced to a voltage or current form. The RIO will contain digital-to-analog converters, analog and digital comparators, counters, programmable timers, and a smart digital interface to perform local control actions. This smart device can find many applications in spacecraft and instrument systems [13]

A first version of the RIO, focusing on temperatures as well as voltage measurements (the TRIO) is already designed and successfully tested. APL's TRIO chip is distributed throughout the X2000 bus (see Figure 1) to measure temperatures with PRTs. The X2000 spacecraft typically needs a total of about 170 temperature measurements. TRIO bare die, in the parallel readout mode, will also be used in the microcontroller included in several spacecraft systems (Optical Communications Controller, Power Controller, etc.). In addition to temperatures, TRIOs will be used with pressure sensors in the propulsion system, and for radiation dose profile measurements throughout the spacecraft. This last function is important for the Europa mission [10].

A die map of the TRIO device is shown in the top panel of Figure 2. The chip is fabricated in a 0.8µ

radiation-hardened CMOS process, operates from a single unregulated power supply of 3-6V, and dissipates 5mW of power at 3V. Both APL and JPL will use hundreds of these chips in their new lightweight, small spacecraft.

### 3. VLSI ASICs Enabling Lightweight Instruments

There is a broad family of science instruments that

compact and low-power electronics [1, 8, 9, 11, 12, 14].

APL's 0.5W, < 0.5 kg compact Energetic Particle Sensor (EPS), being developed under a NASA's Planetary Instrument Definition and Development Program (PIDDP), is presented as an example [6, 7]. The instrument uses Time Of Flight and Energy measurements, to discriminate >10keV ion species in four mass categories and eight energy bands. A schematic block diagram describing the principle of operation (top

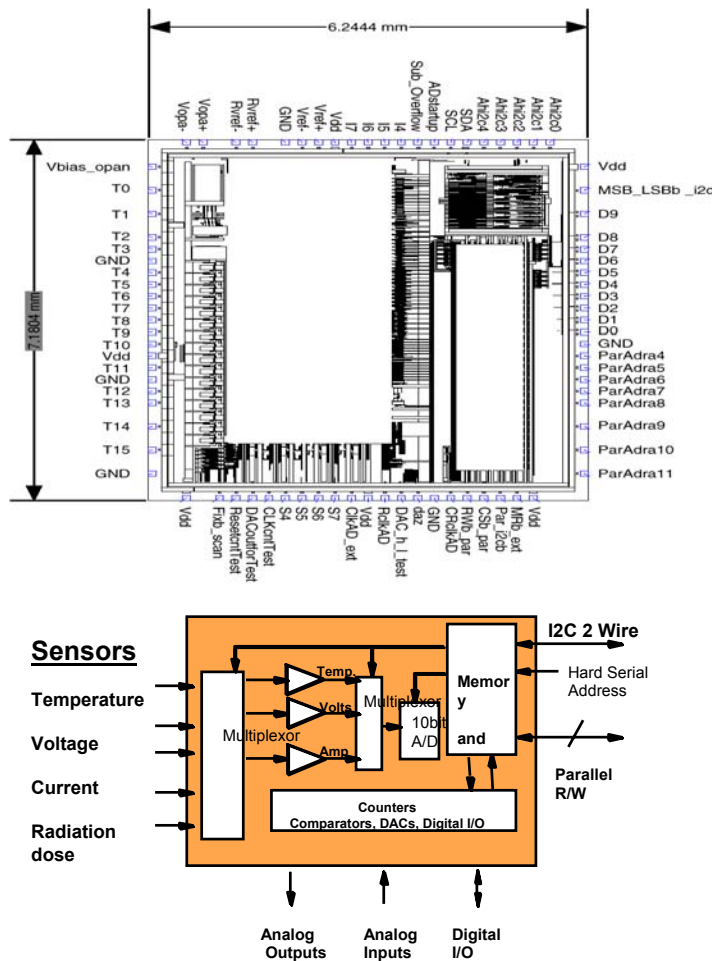


Figure 2: Block diagram of the APL RIO chip (bottom), and die map of the TRIO version (top).

can greatly benefit by the use of ASICs. These include energetic particle and plasma instruments, magnetometers, wave instruments, x-ray and gamma-ray spectrometers, multispectral imagers, etc. Few chips (TOF, Energy, Discriminators), with generic use in many types of instruments, can replace whole electronics boards of standard designs, thus enabling

panel), the mechanical housing (bottom left) and Chip On Board (COB) electronics assembly (bottom right), are shown in Figure 3.

Energetic particles enter the detector head, from a ~180 deg opening through a collimator. Particles penetrate a thin foil in the front and hit an assembly of six Solid State Detectors (SSDs) in the back. Secondary electrons produced in the front and backs foils are

electrostatically focused on corresponding start and stop microchannel plate (MCP) anodes. Processing of the MCP start-stop time difference gives the speed of a particle, and processing of the total charge released in a SSD gives the total energy deposited by a particle. Particle mass and energy is determined by combining the TOF and energy measurements. In addition, the particular SSD ID provides angular resolution. The critical microelectronics technologies enabling a compact and low power implementation, are the Energy and TOF chips.

The Energy chip will give a digital read out of the energy deposited by particles hitting each SSD. The chip will include a low noise Charge Sensitive Amplifier (CSA) with external JFET option, a shaping amplifier, a baseline restorer, a peak detector, a 12-bit analog-to-digital converter, commandable threshold discriminators, and logic [12]. The target is to measure the energy with noise resolution <4 keV FWHM and <20mW of power. Each Energy chip should need minimum external components, in order to be mounted behind its

corresponding SSD, for a compact configuration [11].

The TOF chip will give a digital read out of the start-stop time difference produced by the corresponding start-stop MCPs to infer the particle speed. A sub-nanosecond time resolution is required for good mass discrimination of ions in the energy range 10keV-4MeV. In addition the power dissipation should be kept low. Typically, conventional systems achieving the required time resolution, consume ~1W of power and occupy ~20x20cm double-sided PCB board. The TOF chip achieves a better time resolution, with <30mW of power and occupies a few square cm of area. A radiation-hardened version of the TOF chip is already developed and space qualified for use in the High Energy Neutral Atom (HENA) instrument of the NASA IMAGE mission.

Figure 4 shows the block diagram (bottom) and the die map (top) of the TOF chip. The chip includes two channels of Constant Fraction Discriminators (CFDs) and one Time-to-Digital Converter (TDC). Each CFD channel interfaces to the start or stop MCP, with external bipolar transistors, for matching as well as protection [11].

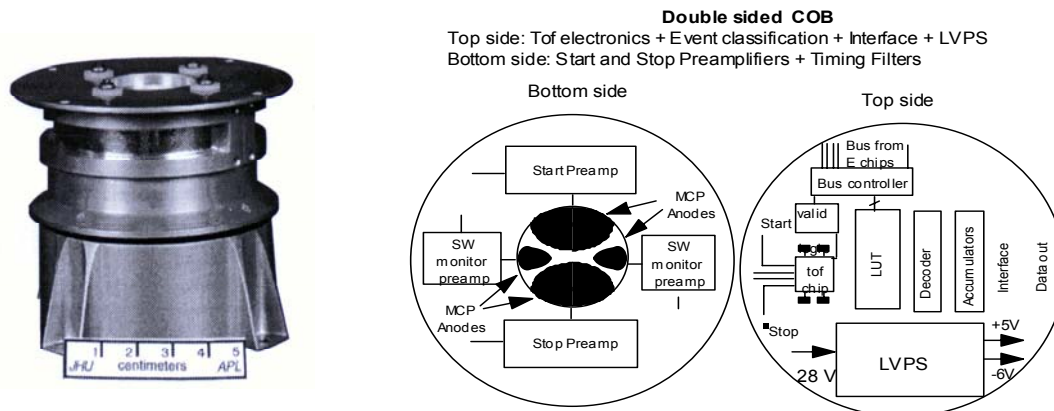
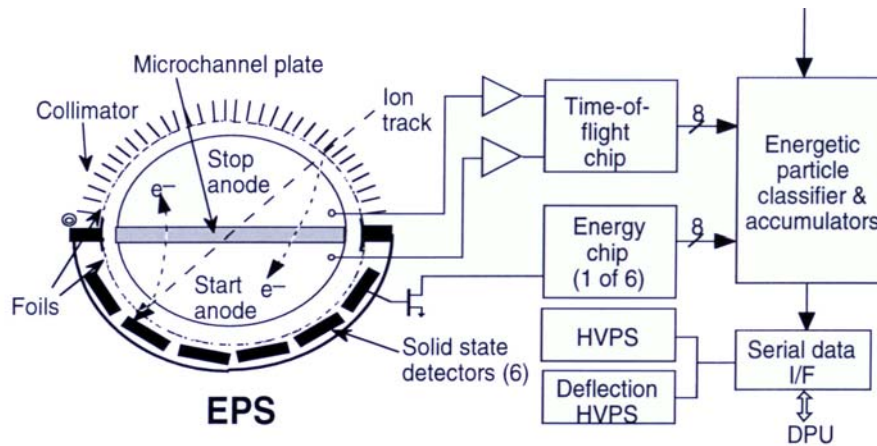


Figure 3: Simplified block diagram (top), mechanical housing (bottom left), and COB

The function of the CFD is to compensate for signal amplitude variations caused by the number of the secondary electrons (1 to 80 depending on the particle species and energy) thus minimizing the time walk of a leading edge discriminator, while introducing a minimum time jitter. The measured time walk of the CFD in a 1-80 dynamic range is  $\sim 200\text{ps}$ , yet the power dissipation per channel is  $< 10\text{mW}$ .

The function of the TDC is to digitize the start-stop time difference with high time precision, to reject non-valid events (multi start-stop conditions etc.), and to provide a digital readout [14]. The TDC digitizes the time

pulses produced by the CFD in 11-bits. The maximum time interval,  $T_{\text{max}}$ , and, consequently, the time digitization step (LSB), is set through a built in Delay Locked Loop (DLL) by an external time reference. The DLL also stabilizes the TDC against temperature, power supply, and total radiation-dose-induced errors.  $T_{\text{max}}$  is settable in the range  $\sim 0.1\mu\text{s}$  to  $5\mu\text{s}$ , which corresponds to a digitization step of  $\sim 50\text{ps}$  to  $2.5\text{ns}$ . Typical noise standard deviation is  $\sim 0.5\text{LSB}$  and typical differential non-linearity is within  $\pm 0.5\text{LSB}$ . TDC operates from an unregulated single power supply of 3-6V at high event rates with a power consumption of few mW, at least an

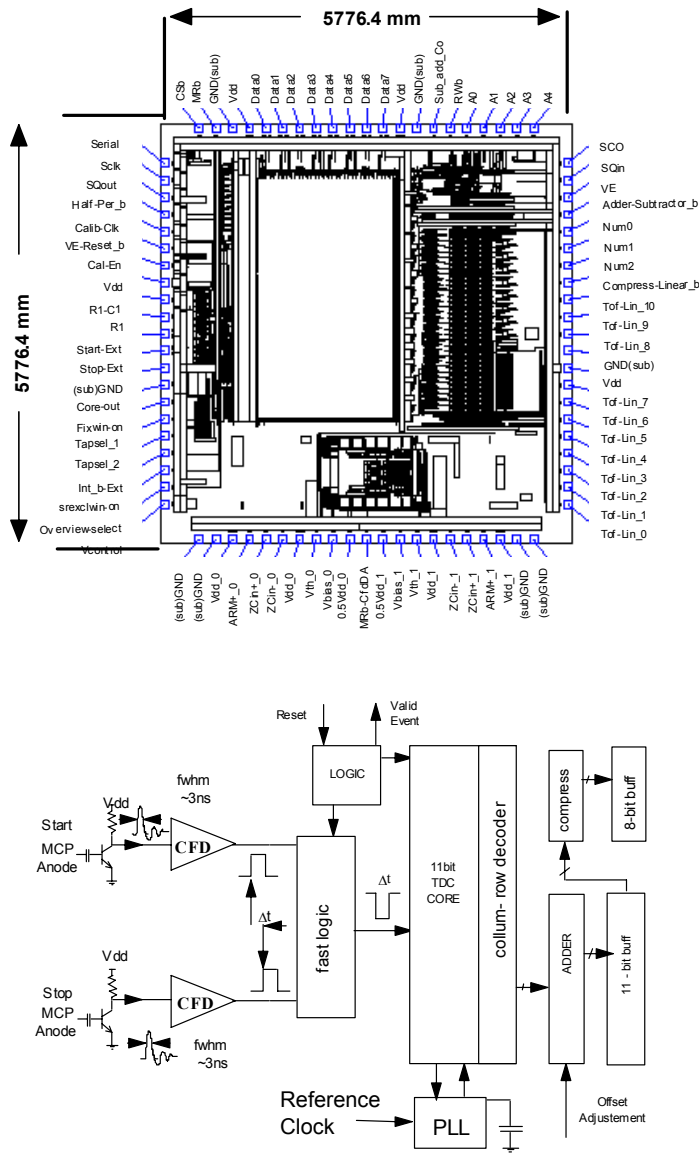


Figure 4: The Time of Flight chip block diagram (bottom) and the chip die map (top).

difference between the rising edges of the start-stop

order of magnitude less than currently used systems in most space instrumentation.

The TOF chip can be used in several modes: as stand alone CFDs, TDC, or combination of the two functions.

than  $\sim 0.6$  LSB = 180ps. Figure 6 shows the power dissipation of the TDC versus event rate and digitization step. It can be seen that for event rates  $< 100$ kHz and digitization  $\sim 300$ ps, the power dissipation is  $< 5$ mW.

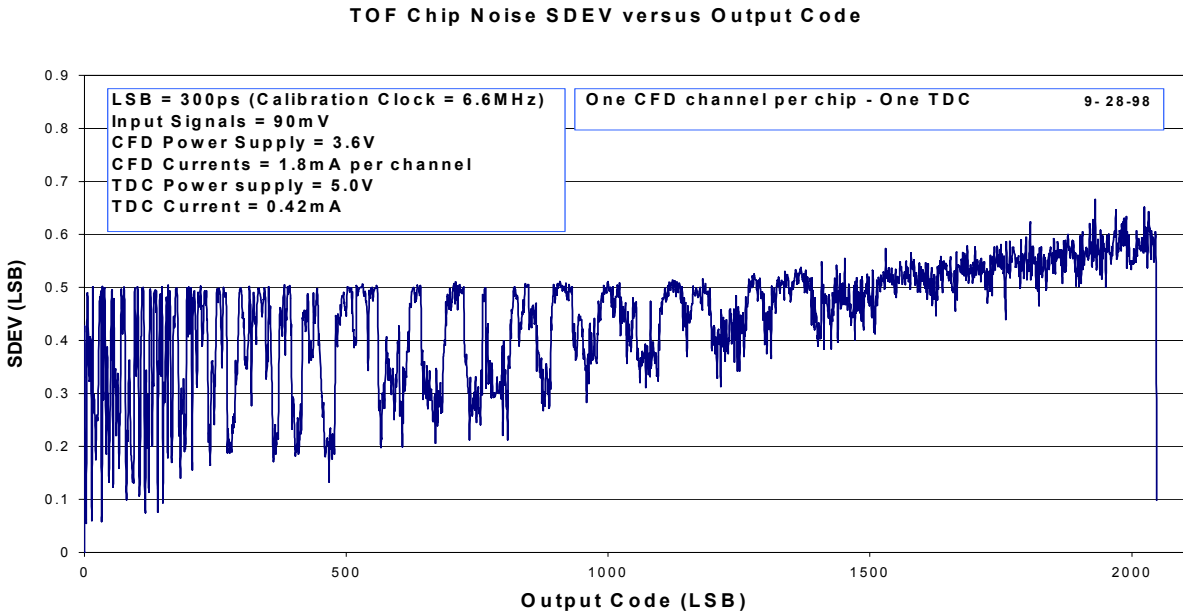


Figure 5: TOF chip time jitter standard deviation normalized in LSB as a function of code

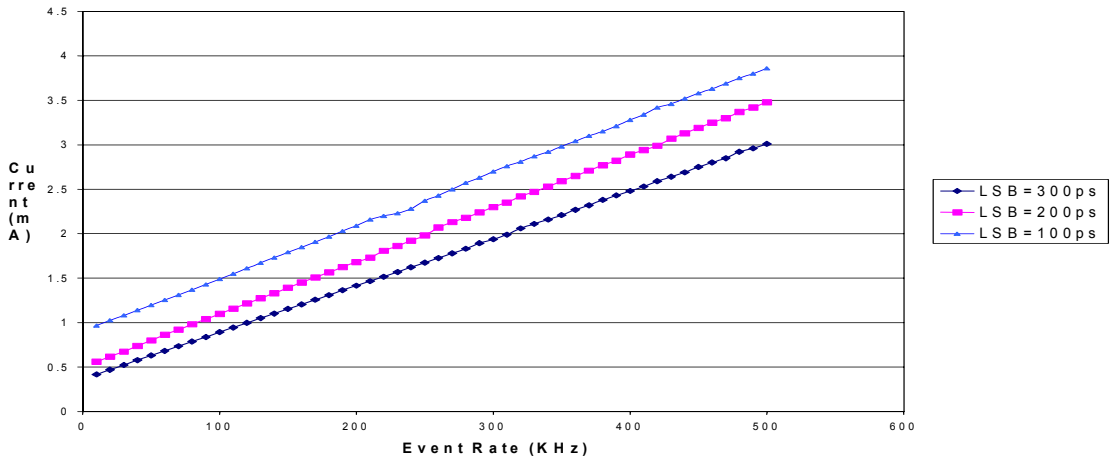


Figure 6: TDC maximum power dissipation as a function of event rate and time digitization.

Figures 5 and 6 shows some measured performance. Figure 5 shows the time jitter standard deviation with respect to output code of the complete CFD-TDC combination. Signal and bias conditions are indicated in the inset; analog signal peak  $\sim 90$ mV, 1.8mA at 3.6V power supply per CFD channel, TDC digitization  $\sim 300$ ps, event rate  $\sim 10$  kHz and TDC power supply 5V. It can be seen that the timing jitter standard deviation remains less

The overall performance of the TOF chip far exceeds any reported conventional design performance in terms of power versus power dissipation as well as size. The chip readily meets the specifications for the compact particle detector as well other types of particle and laser altimetry instruments.

The Energy chip has been fabricated and tested. A channel includes a charge sensitive amplifier, shaper,

peak detector and low-level discriminator. Preliminary noise measurement indicate ~100 e- rms noise with 2pf detector and ~400e- rms with 12pf detector capacitance, at 2micro-seconds shaping time constant. The power dissipation is ~8mW per channel.

#### 4. Conclusions

This paper presented examples of VLSI ASICs developed for spacecraft avionic and space science instrumentation. The products enable a new class of lightweight avionics and instruments with increased performance and low power. It is expected that VLSI technologies and innovative design methodologies such as radiation hard by design will be widely adopted to enable the new challenges of space exploration in the new millennium.

#### 5. Acknowledgements

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