

LOW-VOLTAGE WIDE g_m ADJUSTMENT RANGE, HIGHLY LINEAR BiCMOS OTA

J. Ramírez-Angulo, C. Durbha, G. O. Ducoudray-Acevedo and R.G. Carvajal
jramirez@nmsu.edu, cdurbha@nmsu.edu, gducoudr@nmsu.edu, carvajal@gte.esi.us.es
Klipsch School of Electrical and Computer Engineering
New Mexico State University,
Box 30001, Dept. 3-0, Las Cruces New Mexico, 88003-0001

Abstract. A very low distortion low-voltage BiCMOS OTA with very wide g_m adjustment and input range is presented. It is based on a highly linear voltage-to-current converter input stage and it uses linear electronically programmable current mirrors to achieve wide transconductance gain adjustment range. It can be implemented in BiCMOS technology or standard CMOS technology with lateral bipolar transistors or MOS transistors operating in subthreshold. The OTA input range remains approximately constant with g_m adjustment. Bandwidth and input signal range can be adjusted independently of g_m . Simulation results in $1.5\mu\text{m}$ CMOS technology with $\pm 0.9\text{V}$ supplies and 1V input range are presented which confirm the characteristics of the proposed structure.

I. INTRODUCTION

Due to its versatility, the operational transconductance amplifier (OTA) is a very important building block of analog VLSI circuits. It is used to implement continuous-time linear and nonlinear VLSI circuits with programmable characteristics [1]-[4]. Some key features for practical applications of the OTA are:

1) a wide range of (transconductance) gain adjustment¹. Gain programmability allows to compensate for large IC fabrication tolerances and for temperature variations. This characteristic also allows implementation of systems with wide range programmable characteristics,

2) a highly linear transconductance characteristic, this

¹The gain of an OTA, as opposed to the gain of an op-amp, forms integral part of the circuit design equations

is required since the OTA is used in open loop structures with large differential input signals.

3) Operation with low supply voltage. This is a requirement imposed by modern deep submicron CMOS technologies which are expected to operate with sub-volt ($<1\text{V}$) single supplies within the next few years.

4) High input signal swing (with low distortion). In modern technologies input swing should be comparable to the supply voltage for maximization of the dynamic range in a low supply environment

Other important practical aspects are: a) low power dissipation for mobile and wireless applications, b) constant performance characteristics (bandwidth, output resistance, distortion over the g_m (transconductance gain) adjustment range and c) linear control over g_m to relax the requirements and complexity on the control (tuning) circuitry for a system based on OTAs.

Traditionally, OTA linearization has taken place by linearizing the input differential pair (DP) [6]-[9], [11][12],[14] so that either a linear difference I_1-I_2 (I_1 and I_2 being the DP transistor currents) or both linear I_1 and I_2 are generated. These currents are typically scaled by mirrors with gain A and the difference $A(I_1-I_2)$ is available as the OTA output current, using an additional mirror. Adjustment of the transconductance gain takes place in this approach by adjustment of the DP gain (g_{md}).

Drawbacks of this approach where both linearization and g_m control take place on the DP are: 1) most of the OTA performance characteristics (input range, BW, noise, offset, distortion ..) change drastically with adjustment of g_{md} , 2) In CMOS structures the gain adjustment range is very limited (practically 2

octaves), 3) most of the proposed approaches are not appropriate for operation with low supply voltages. In bipolar circuits g_m can be adjusted over a very wide range of values (several decades) but the maximum input signal range is very small (a few mV). Emitter (source) degeneration techniques are used to alleviate this problem. The use of emitter (or source) degeneration to linearize the DP and increase its input range leads to fixed (non programmable) DP gain g_{md} . Source degeneration techniques based on voltage followers and resistors or MOS transistors operating in triode mode have been reported [9], [15]. These are characterized by significant nonlinear distortion and very limited input range. This is imposed by the condition to keep MOS transistors in ohmic mode of operation. Distortion is related to the fact that conventional MOS voltage followers used with source degeneration techniques followers are subject to large drain current changes and as a consequence nonsymmetrical gate-source voltage changes takes place. And the input differential voltage is transferred with some distortion to the source degeneration device

In this paper we report a new low-voltage very wide range g_m adjustable, highly linear OTA. It is based on a CMOS low-voltage wide input range, highly linear current to voltage conversion input stage. This is used in combination with linear gain programmable current mirrors in order to achieve a very wide range continuously adjustable gain. Programmable current mirrors are based on translinear loops and they can be implemented using vertical bipolar transistors in a BiCMOS process. They can also be implemented using lateral bipolar transistors or MOS transistors operating in subthreshold in a mainstream CMOS process. The proposed circuit has a very wide input range which is comparable to the supply voltage and the input range and bandwidth remain approximately constant with gain adjustment.

II. NEW LOW-VOLTAGE WIDE ADJUSTMENT RANGE LINEAR OTA

Input voltage to current transformation stage: Fig. 1 shows the scheme of the proposed OTA. The linear voltage to current conversion stage has two buffers and a resistor R. The input buffers are formed by M1, Q2 and Q3 and M1P, Q2P and Q3P. They have very low output impedance $R_{out}=1/g_{m1}(g_{m2}r_{o2})$ on the order of a few Ohms (g_{mi} and r_{oi} are transconductance gains and output resistances of M_i or Q_i respectively). These buffers are a modified version of a circuit that some of the authors have denoted “flipped voltage follower” [16] which has a

wide input range and low supply requirements. The supply requirements of each of the input buffers of the circuit of Fig. 1 is given by $VDD_{MIN}=2V_{BE} + V_{DSsat}$ (V_{BE} is a base-emitter voltage drop, V_{DSsat} an MOS drain-source saturation voltage). VDD_{MIN} can be as low as 1.5V. The buffer’s maximum peak-to-peak input signal swing is expressed by $V_{ippMAX}=2V_{BE}-V_{DSsat}-V_{CEsat}$ and can be as high as 1.2V. (V_{CEsat} is the collector emitter saturation voltage). The buffers are used to transfer the differential input voltage $V_d=V_{i+}-V_{i-}$ to the resistor terminals connected between the (low impedance) output nodes of the input buffers. This generates a signal current $I_{in}=V_d/R$. The voltage to current transformation is highly linear due to the fact that V_d is transferred without distortion to R. This is due to the fact that the gate-source drop in M1, M1P is constant and the impedance at the sources of M1, M1P is very low

Current gain stage: Transistors Q2-Q7 and Q2P-Q7P form translinear loops and they are used to implement linear programmable current mirrors [17]-[18] with current gain $A=I_{dir}/I_{inv}$. This gain has two degrees of freedom: the DC bias currents I_{dir} and I_{inv} . Straightforward analysis using the translinear principle [10], [13] shows that currents I_B and I_{BP} in Fig. 1 can be expressed by $I_B=I_A(I_{dir}/I_{inv})$ and $I_{BP}=I_{AP}(I_{dir}/I_{inv})$ respectively (Currents I_A and I_{AP} are given by: $I_A=I_b-I_{in}$ and $I_{AP}=I_b+I_{in}$). Transistors M9-M10 (and M9P-M10P) form a conventional MOS mirror which generates an output current $I_{out}=I_A-I_{AP}=2I_{in}(I_{dir}/I_{inv})$. This can be expressed by

$$I_{out}=G_m V_d$$

Where $G_m=2(I_{dir}/I_{inv})/R$

Remarks:

- The structure of Fig. 1 overcomes some of the limitations discussed in section I.
- All currents I_A and I_{AP} as well as I_B and I_{BP} are linear and symmetrical. They are given by $I_B=(I_b-V_d/R)(I_{dir}/I_{inv})$ and $I_{BP}=(I_b+V_d/R)(I_{dir}/I_{inv})$ respectively. In most CMOS linearizing schemes each current (I_1 and I_2) has large nonlinear components which are common to I_1 and I_2 . These are cancelled using a current mirror to generate the difference $I_{out}=I_1-I_2$. In these linearizing schemes mismatch errors cause incomplete cancellation of nonlinear terms and lead to nonlinear distortion. In the here proposed

scheme mismatch does not lead to distortion and availability of linear symmetrical currents allow easy implementation of fully differential linear OTAs .

- The transconductance gain $G_m=2(I_{dir}/I_{inv})/R$ has a very wide range programmability in terms of the bias currents I_{dir} and I_{inv} and it is approximately temperature independent (This assumes R has a low TCR)
- The maximum input range of the circuit of Fig.1 is given by $V_{d_{MAX}}=I_b R$. This range remains constant with gain adjustment and it can be programmed independent of the gain g_m with I_b .
- Translinear loops have been used for implementation of wide range programmable OTAs [17]-[19]-[21] . Most of the previously reported implementations have lacked a voltage to current conversion input stage that remains highly linear over a wide input range and that operates on a low supply voltage.
- An all MOS version of the circuit of Fig. 1 can be implemented in mainstream CMOS technology with MOS transistors operating in subthreshold. In this case bipolar transistors (Q2-Q7 and Q2P-Q7P) can be replaced directly by MOS transistors. MOS transistors in subthreshold are also governed by exponential equations similar to bipolar transistors. Implementation of translinear cells in CMOS circuits in subthreshold has been reported by several authors.
- Given that (as indicated above) there are two degrees of freedom (I_{dir} and I_{inv}) for adjustment of the transconductance gain the OTA of Fig. 1 has additional flexibility and versatility for many applications. One example is for the implementation of wide range tunable OTA-C filters with independent and linear adjustable center frequency, quality factor and gain.
- The bandwidth of the circuit of Fig. 1 is determined mainly by the poles of the section formed by M8,M9,M10 and M8P,M9P and M10P. In order to reduce current variations in this section and maintain the OTA bandwidth approximately constant with gain adjustment two current sources with values I_{bsh} (shown with broken lines in Fig. 1) can be added

optionally to the circuit of Fig. 1.

- A fully differential version of the circuit of Fig. 1 is shown in Fig. 2a. This makes use of gain dependent DC current sources with value $A I_b$. Fig. 2b shows the bias circuit for generation of these sources. This circuit uses a translinear circuit formed by Q2B-Q7B.

III. SIMULATION RESULTS

The circuit of Fig. 1 has been verified with simulations in 1.5 μ m BiCMOS (MOSIS-AMI) technology. Fig. 3 shows simulation results of the DC transfer characteristic with $I_{bias}=70\mu A$, $R=7k\Omega$, $R_L=1k\Omega$, $V_{dd}=\pm 0.9V$, $I_{inv}=100\mu A$ and I_{dir} stepped from $5\mu A$ to $105\mu A$ in $20\mu A$ steps. (NMOS and PMOS transistors have dimensions 100/3 and 250/3 $\mu m/\mu m$ respectively). It can be seen that the input range is close to 1V and the gain remains linear over a very wide adjustment range. Fig. 4 shows simulations of the AC response for the same gain adjustment range and with a load resistor $R_L=1k\Omega$. Fig. 5 shows the transient response for the same gain adjustment range and upon application of a square input pulse. Fig. 6 shows simulations of the transconductance gain with $I_{dir}=I_{inv}=100\mu A$ and I_b stepped from $20\mu A$ to $100\mu A$ in $20\mu A$ steps. It can be seen how the input range (and current saturation levels) can be adjusted independent of the gain Total harmonic distortion for a 100kHz 1V peak to peak input signal with gain setting current $I_{dir}=50\mu A$ was under 0.2%. Fig. 6 shows simulations of the transconductance characteristic of the fully differential OTA of Fig. 2 with two load resistors $R_{L1}=R_{L2}=1k\Omega$ and with similar conditions as in Fig. 3.

IV. CONCLUSIONS

A highly linear OTA structure with very wide g_m adjustment, wide input range and both linear and reciprocal g_m control was introduced and verified. It is based on programmable current mirrors which are linear and continuously adjustable. The proposed circuit is believed to overcome some of the practical limitations of other reported low-voltage linear OTA structures and to provide increased versatility to the OTA as building block of analog VLSI systems.

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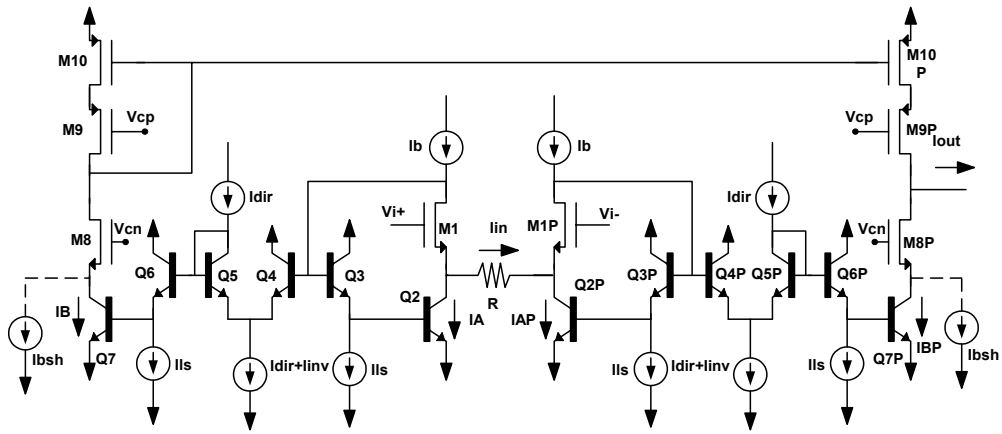


Fig.1 Wide tuning range low-voltage BiCMOS OTA

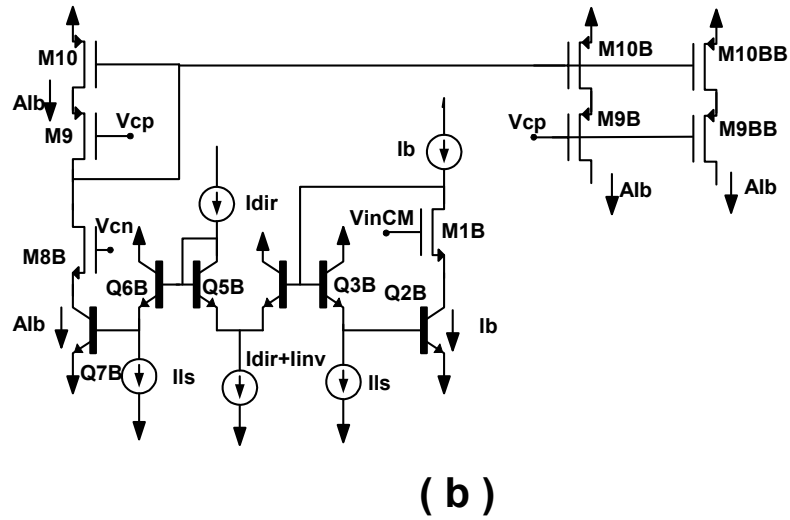
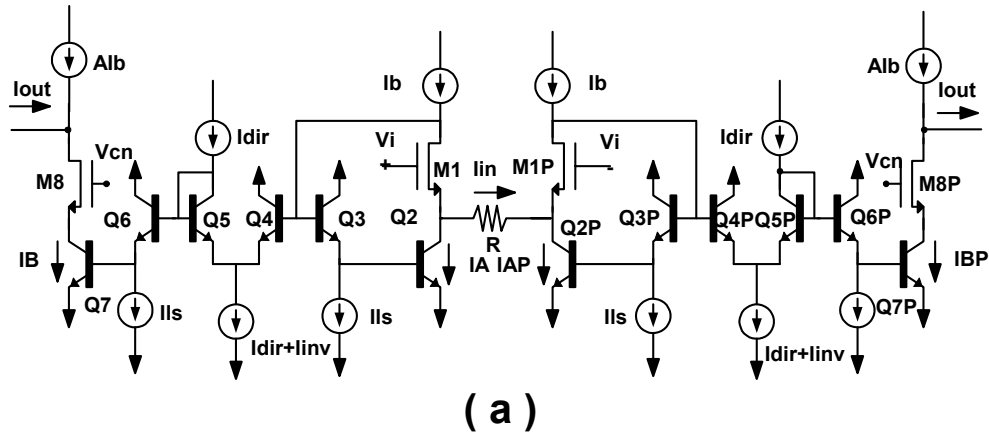


Fig. 2 (a) Fully differential OTA (b) Circuit for generation of bias currents A_{ib}

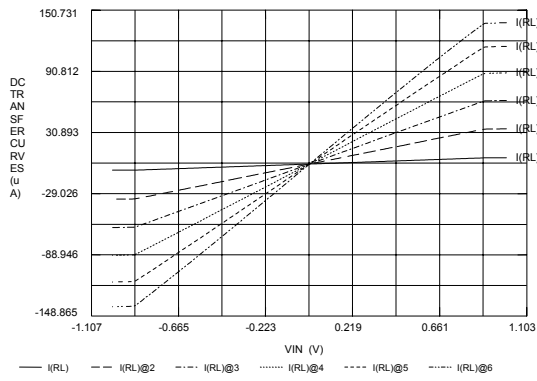


Fig. 3 (a) DC transconductance characteristic of circuit of Fig. 1 for gain setting current I_{dir} stepped from $5\mu\text{A}$ to $105\mu\text{A}$ in $20\mu\text{A}$ steps

**BiCMOS OTA using programmable current mirrors in 1.5um AMIS input stage With FVF linear V to I conversion

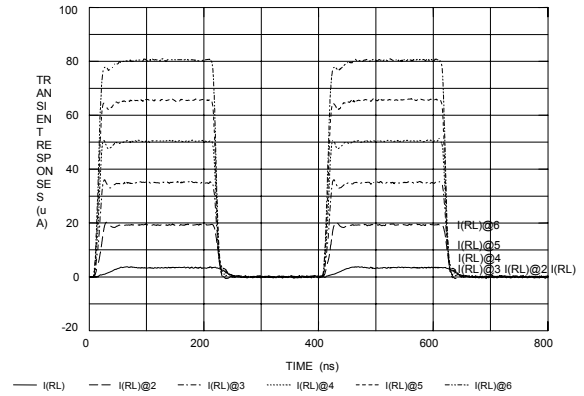


Fig. 5 Transient response of circuit of Fig. 1 for various gain settings

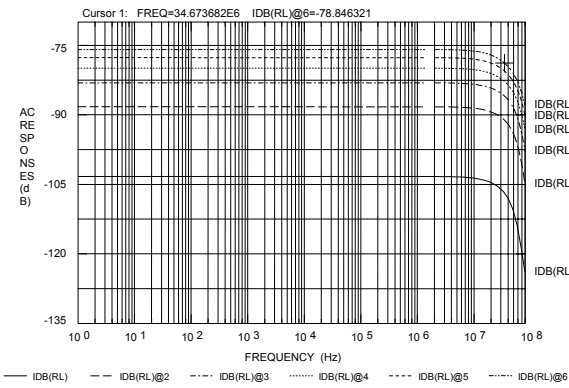


Fig. 4 AC response of circuit of Fig. 1 for various gain settings

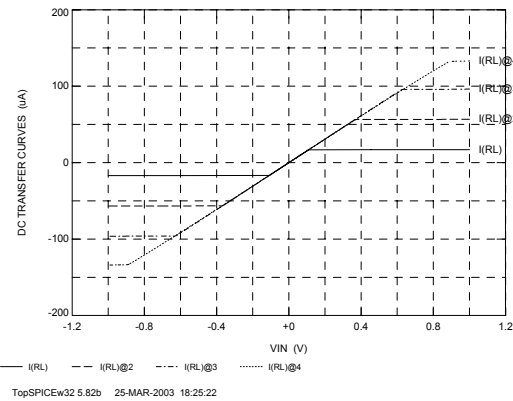


Fig. 6 Input range adjustment: DC Transconductance characteristic of circuit of fig. 1 with I_b stepped from $10\mu\text{A}$ to $70\mu\text{A}$ in $20\mu\text{A}$ steps